



Vienna Electronics Lab



Belle SVD

- ADC readout system
- First stage of track trigger L0
- Hit data for L1.5 trigger processor
- Real-time operation

Vienna Electronics Lab

- Involved since August 2001



M. Pernicka
70%



J. Pirker
30%



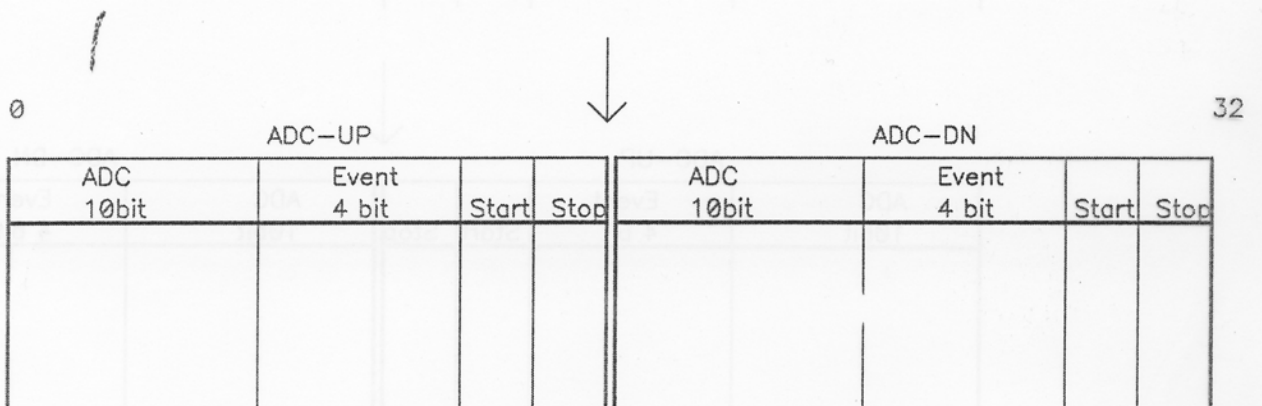
S. Schmid
100%



H. Steininger
80%

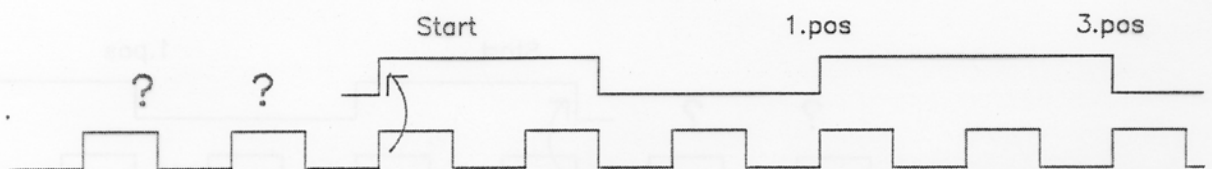
1	n	X	
2	n		
3	n		
3072	n		X
1	n+1	X	

24 Inputs x 128 16bit



③

Information for L1.5 Trigger



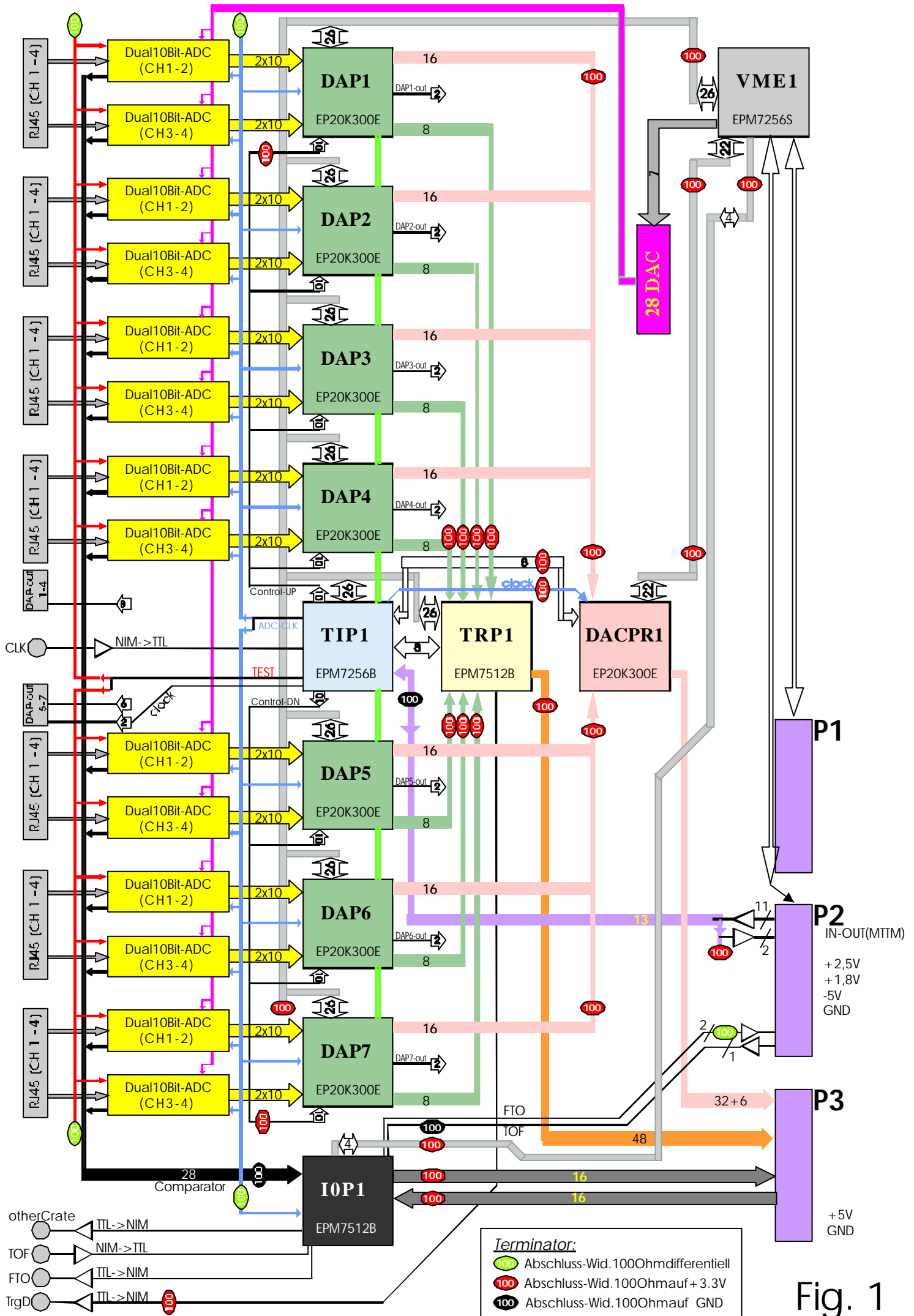


Fig. 1

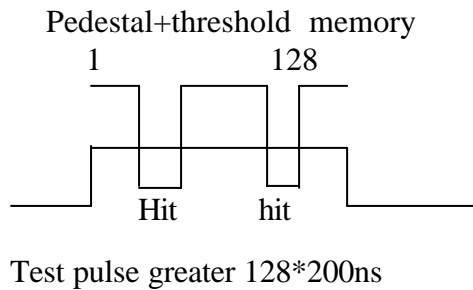
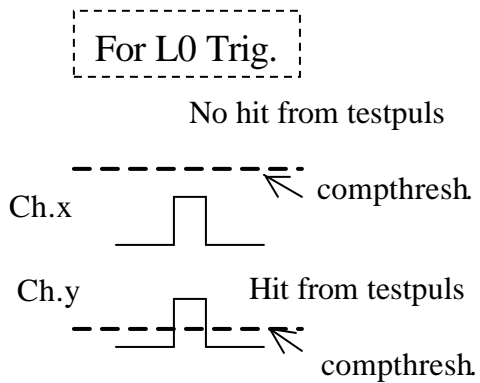
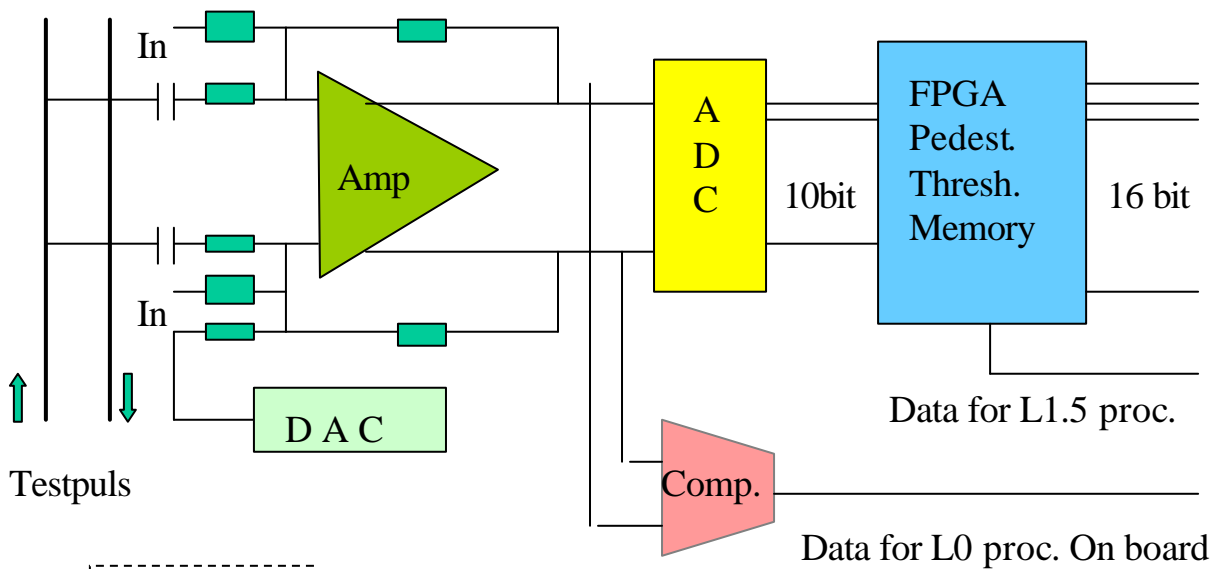
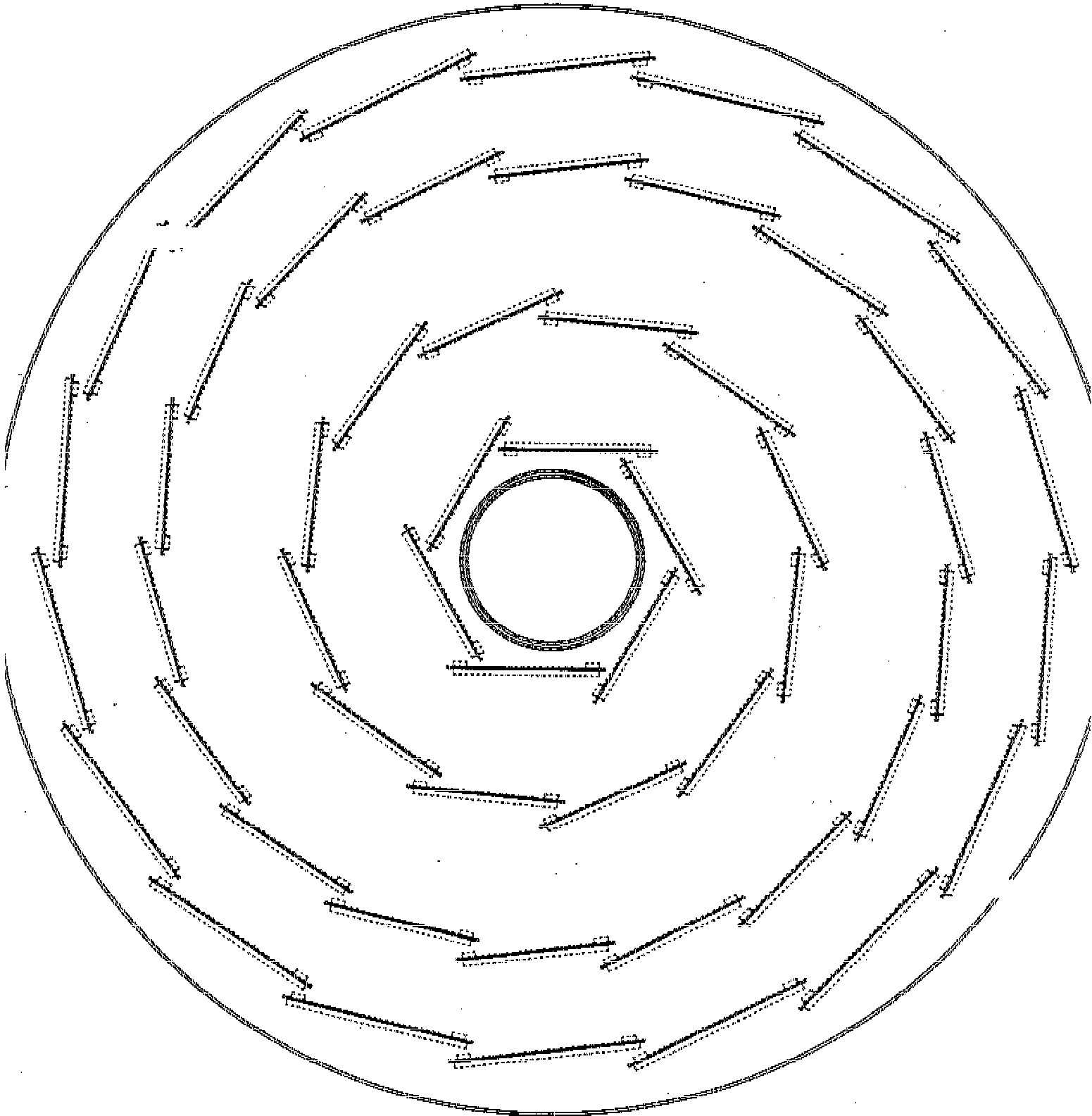


Fig. 3



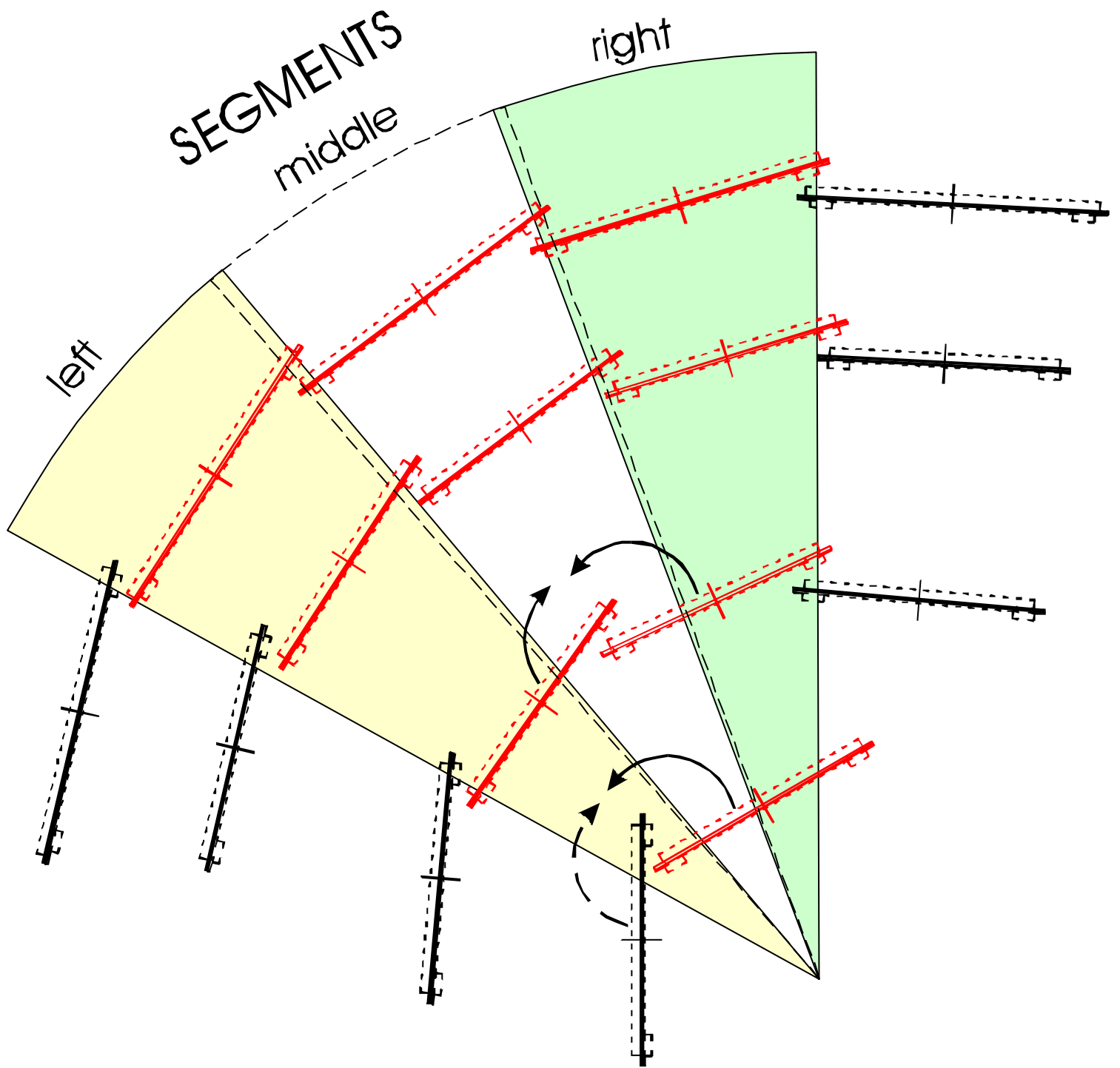
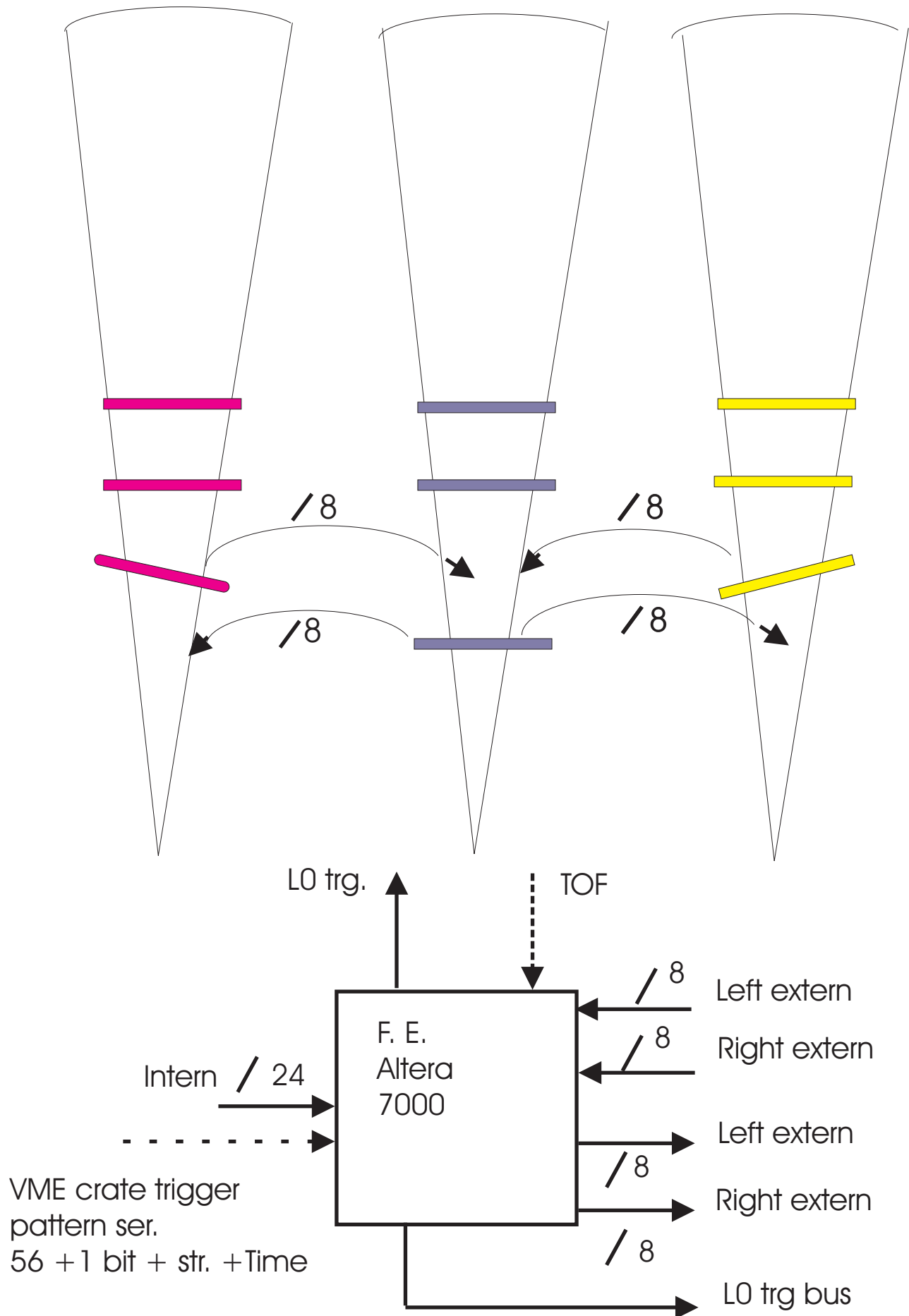
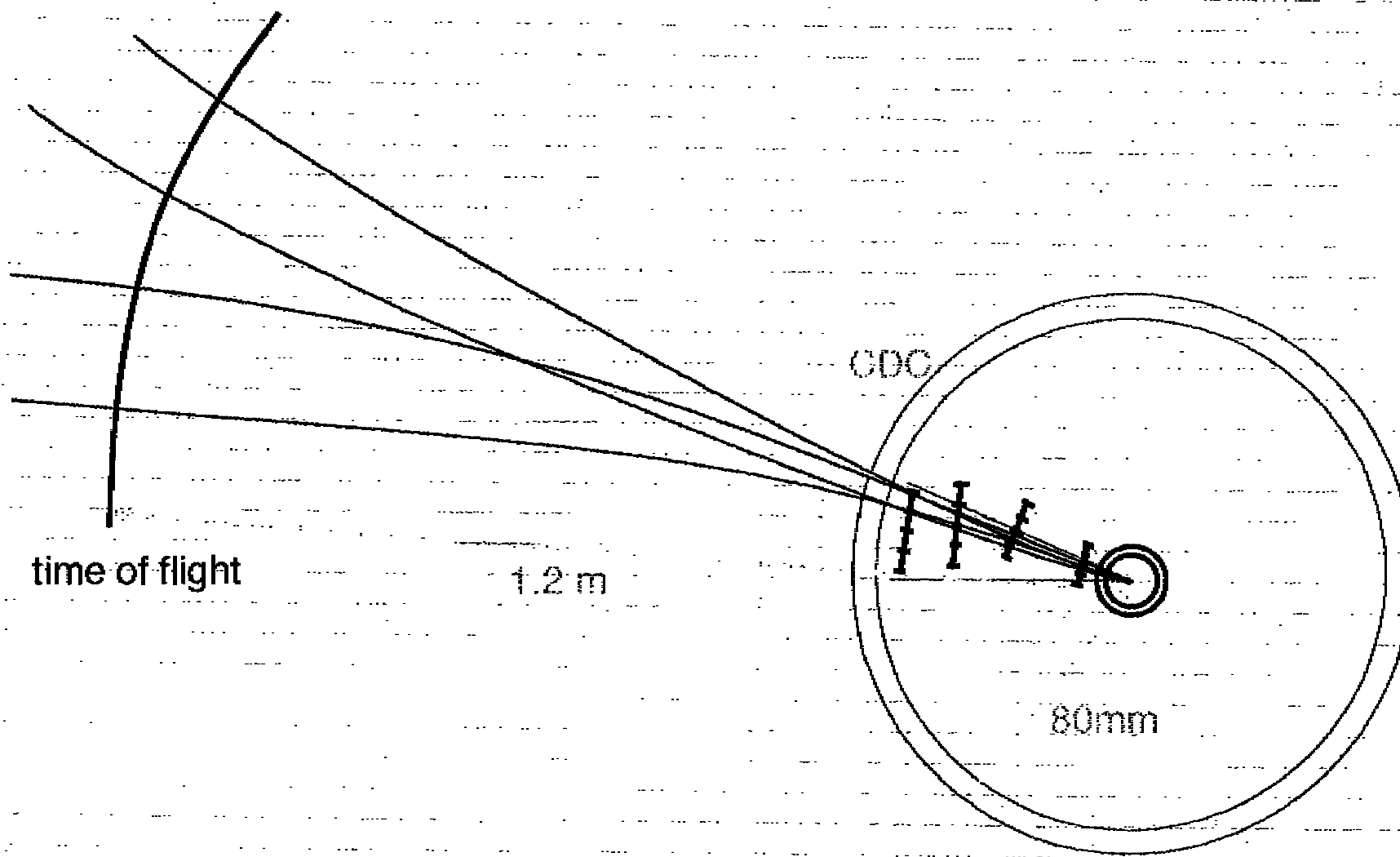


Fig.5

LEFT 1/18 MIDDLE 1/18 RIGHT 1/18

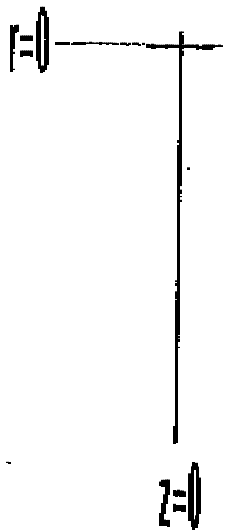


Belle Trigger

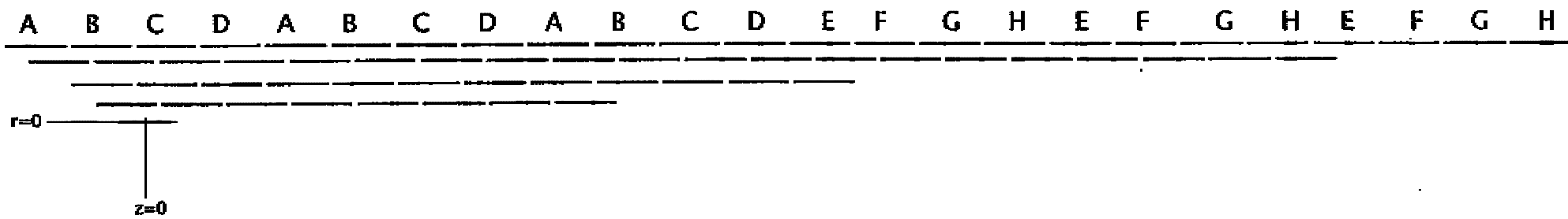


A B C D A B C D A B C D E F G H E F G H E F G H

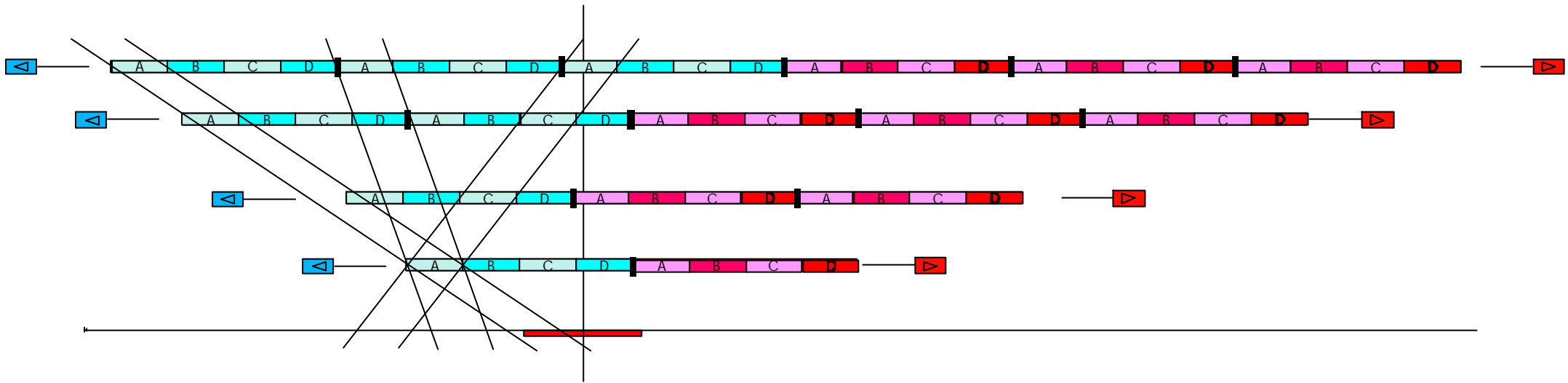
A B C D E F G H



stretched belle by belle_sim_ps or 11.12.2001 pernicka/bauer
contact: thomas.bauer@cern.ch



belle by belle_sim ps on 11.12.2001 pernicka/bauer
contact:thomas.bauer@cern.ch



3 channels for the FASTOR outputs of layer 1/A and layer 4/A
 2 channels are useless and will be not programmed.

Fig.4

BUNCH CROSSING TOLERANCE at $t=0$ $z=0$ +/-30.000000

BELLE TRIGGER CHANNEL SIMULATION
(pernicka/bauer dez.2001) thomas.bauer@cern.ch

L1	L2(%)	L3(%)	L4
A	X(20%) or A(80%)	A (98%) or B(2%)	A
A	A(75%) or B(25%)	A (25%) or B(75%)	B
A	A(41%) or B(59%)	B (51%) or C(49%)	C
A	A(7%) or B(93%)	C (78%) or D(22%)	D
B	B(76%) or C(24%)	B (25%) or C(75%)	C
B	B(41%) or C(59%)	C (52%) or D(48%)	D
B	B(7%) or C(93%)	D (78%) or A(22%)	A
B	C(72%) or D(28%)	D (5%) or A(95%)	B
B	C(38%) or D(62%)	A (32%) or B(68%)	C
B	C(3%) or D(97%)	B (59%) or C(41%)	D
B	D(69%) or E(31%)	C (85%) or D(15%)	A
C	D(38%) or E(62%)	B (32%) or C(68%)	D
C	D(4%) or E(96%)	C (59%) or D(41%)	A
C	E(69%) or F(31%)	D (86%) or E(14%)	B
C	E(35%) or F(65%)	D (13%) or E(87%)	C
C	E(0%) or F(100%)	E (99%) or F(1%)	D
C	F(66%) or G(34%)	F (66%) or G(34%)	E
D	F(35%) or G(65%)	E (13%) or F(87%)	D
D	F(0%) or G(100%)	F (40%) or G(60%)	E
D	G(66%) or H(34%)	G (66%) or H(34%)	F
D	G(32%) or H(68%)	H (93%) or E(7%)	G
D	H(97%) or E(3%)	H (20%) or E(80%)	H
D	H(63%) or E(37%)	E (47%) or F(53%)	E
E	E(97%) or F(3%)	E (20%) or F(80%)	E
E	E(63%) or F(37%)	F (47%) or G(53%)	F
E	E(28%) or F(72%)	G (74%) or H(26%)	G
E	F(94%) or G(6%)	G (0%) or H(100%)	H
E	F(60%) or G(40%)	H (27%) or E(73%)	E
E	F(25%) or G(75%)	E (54%) or F(46%)	F
F	G(94%) or H(6%)	H (1%) or E(99%)	E
F	G(60%) or H(40%)	E (27%) or F(73%)	F
F	G(25%) or H(75%)	F (54%) or G(46%)	G
F	H(91%) or E(9%)	G (81%) or H(19%)	H

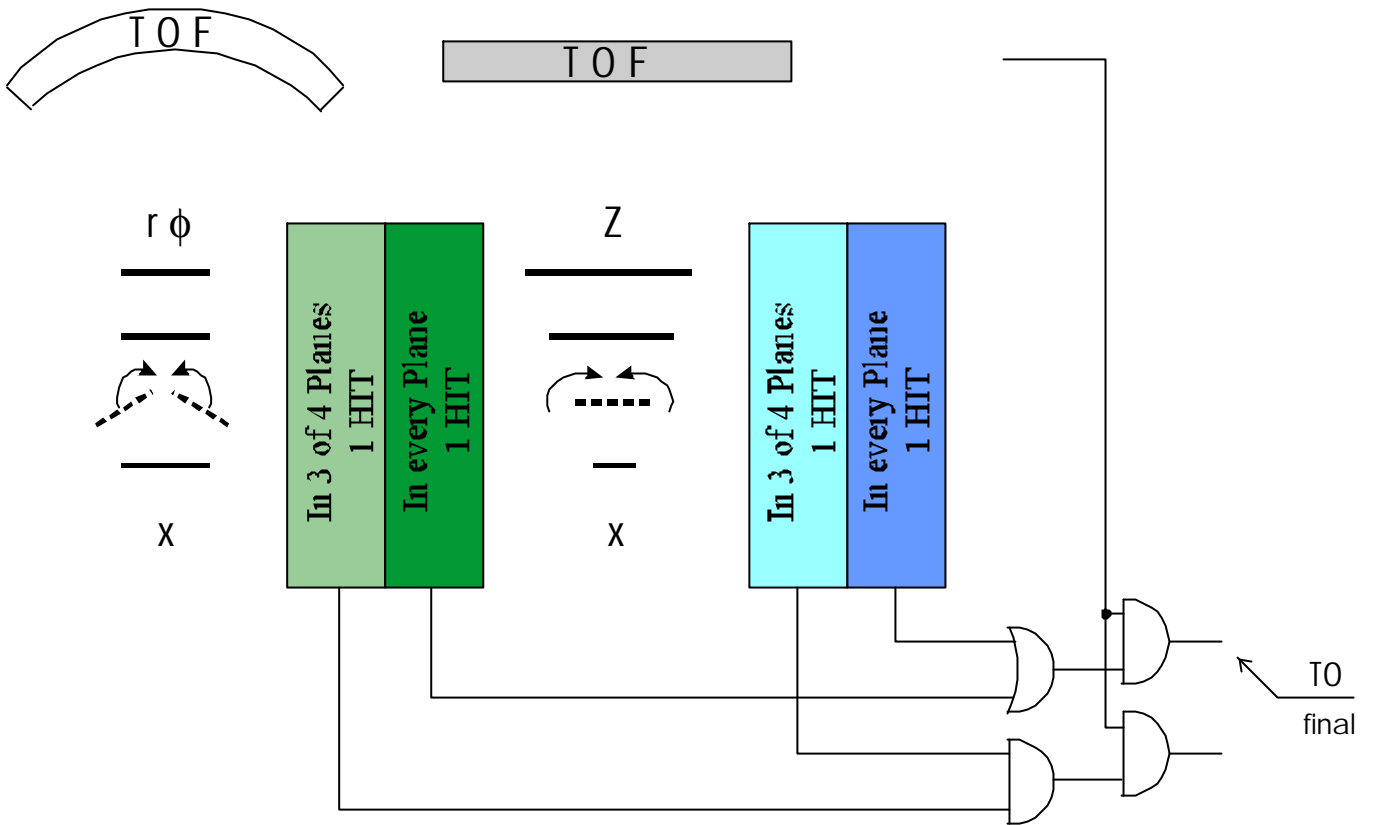
D	F(35%) or G(65%)	E (13%) or F(87%)	D
D	F(0%) or G(100%)	F (40%) or G(60%)	E
D	G(66%) or H(34%)	G (66%) or H(34%)	F
D	G(32%) or H(68%)	H (93%) or E(7%)	G
D	H(97%) or E(3%)	H (20%) or E(80%)	H
D	H(63%) or E(37%)	E (47%) or F(53%)	E
D	H(28%) or E(72%)	F (73%) or G(27%)	F
E	H(32%) or E(68%)	E (93%) or F(7%)	H
E	E(97%) or F(3%)	E (20%) or F(80%)	E
E	E(63%) or F(37%)	F (47%) or G(53%)	F
E	E(28%) or F(72%)	G (74%) or H(26%)	G
E	F(94%) or G(6%)	G (0%) or H(100%)	H
E	F(60%) or G(40%)	H (27%) or E(73%)	E
E	F(25%) or G(75%)	E (54%) or F(46%)	F
F	G(94%) or H(6%)	H (1%) or E(99%)	E
F	G(60%) or H(40%)	E (27%) or F(73%)	F
F	G(25%) or H(75%)	F (54%) or G(46%)	G
F	H(91%) or E(9%)	G (81%) or H(19%)	H

BUNCH CROSSING TOLERANCE at $t=0$ $z=0$ +/-40.000000

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A	A(41%) or B(59%)	B (51%) or C(49%)	C
A	A(7%) or B(93%)	C (78%) or D(22%)	D
A	B(72%) or C(28%)	C (5%) or D(95%)	A
B	B(76%) or C(24%)	B (25%) or C(75%)	C
B	B(41%) or C(59%)	C (52%) or D(48%)	D
B	B(7%) or C(93%)	D (78%) or A(22%)	A
B	C(72%) or D(28%)	D (5%) or A(95%)	B
B	C(38%) or D(62%)	A (32%) or B(68%)	C
B	C(3%) or D(97%)	B (59%) or C(41%)	D
B	D(69%) or E(31%)	C (85%) or D(15%)	A
C	D(72%) or E(28%)	A (5%) or B(95%)	C
C	D(38%) or E(62%)	B (32%) or C(68%)	D
C	D(4%) or E(96%)	C (59%) or D(41%)	A
C	E(69%) or F(31%)	D (86%) or E(14%)	B
C	E(35%) or F(65%)	D (13%) or E(87%)	C
C	E(0%) or F(100%)	E (99%) or F(1%)	D
C	F(66%) or G(34%)	F (66%) or G(34%)	E

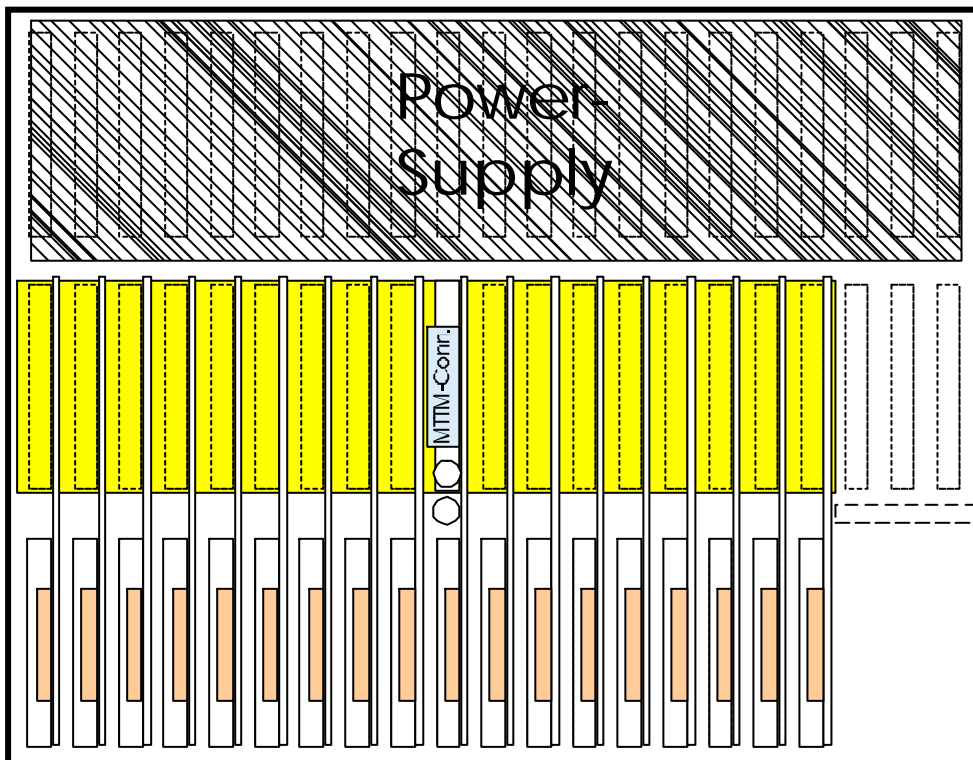
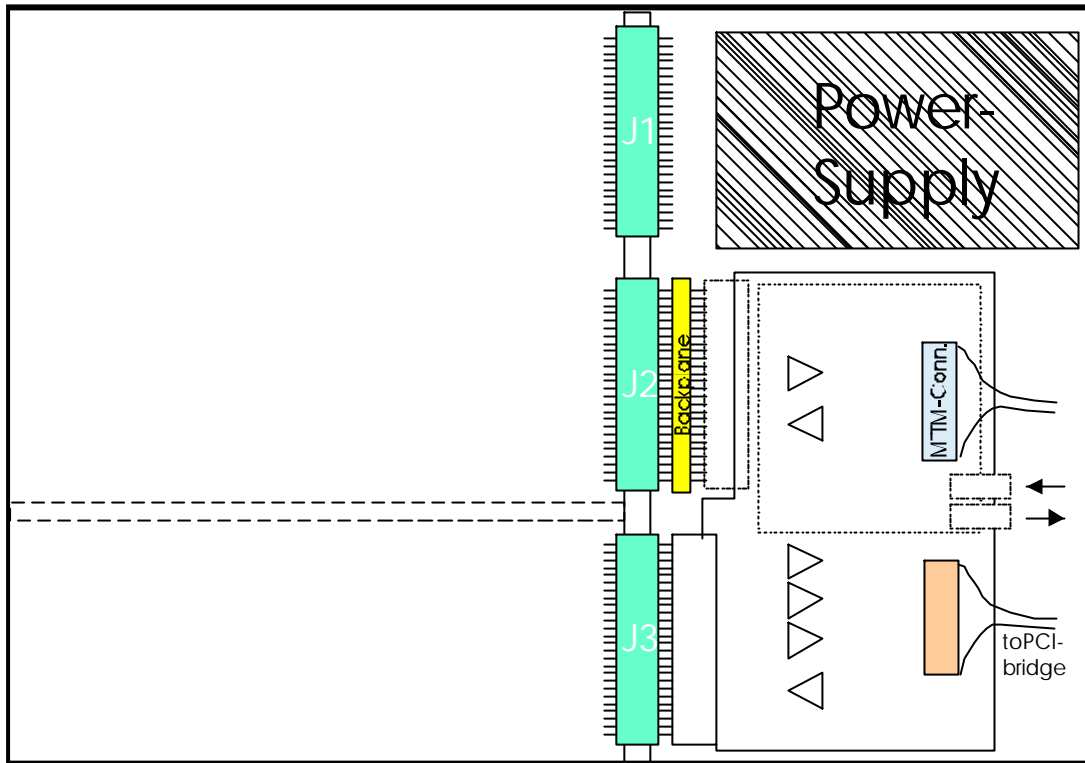
T O F Segment



--- modul which is read out from left or right neighbour modul
 (f.i. final trigger logic for a middle segment)

Fig.6

Side-View



Rear-View

Fig.7

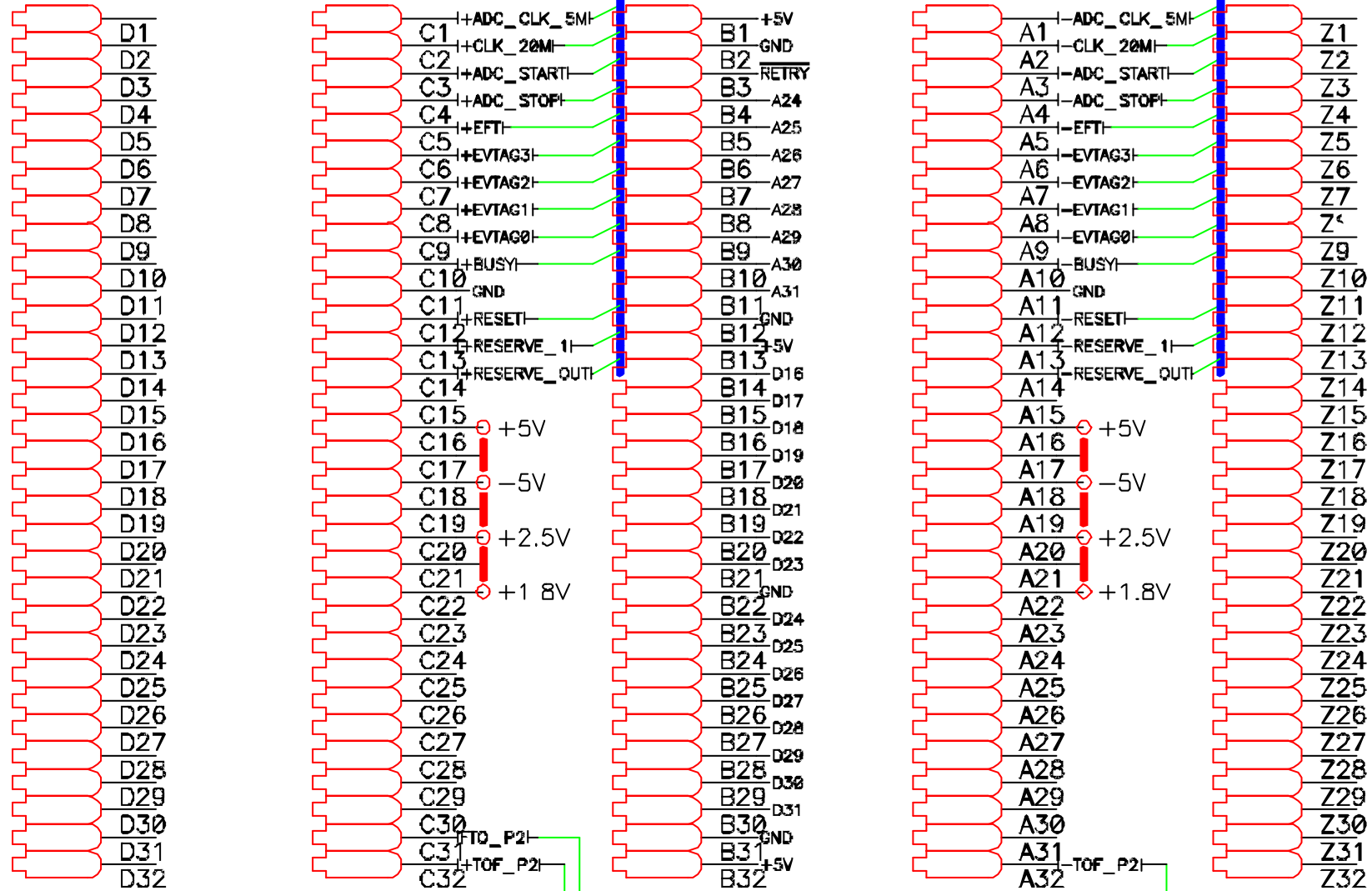
parallel bus for MTTM signals

112 (128)

P2

P2

VME-Connector 160pin

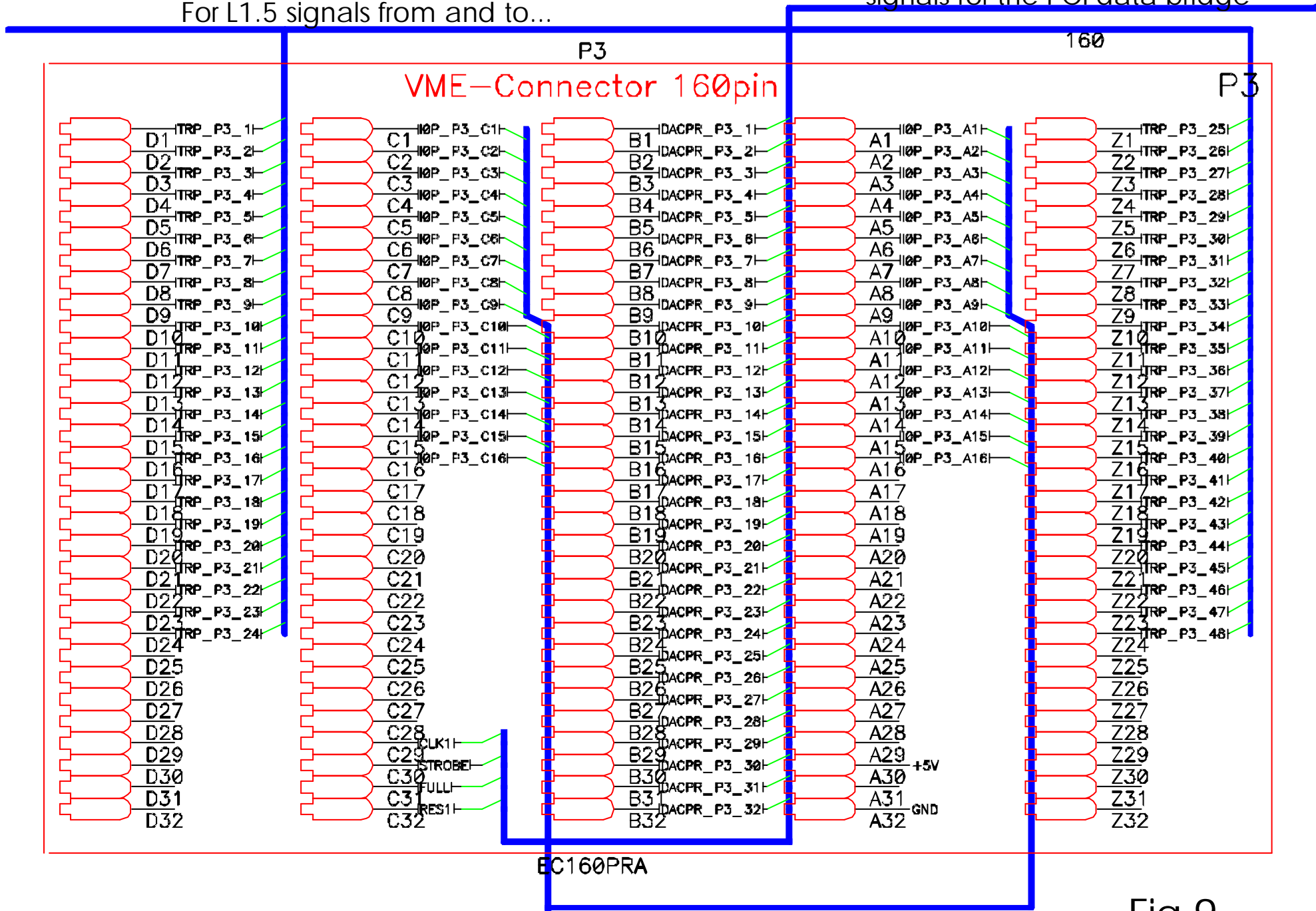


EC160PRA

Fig.8

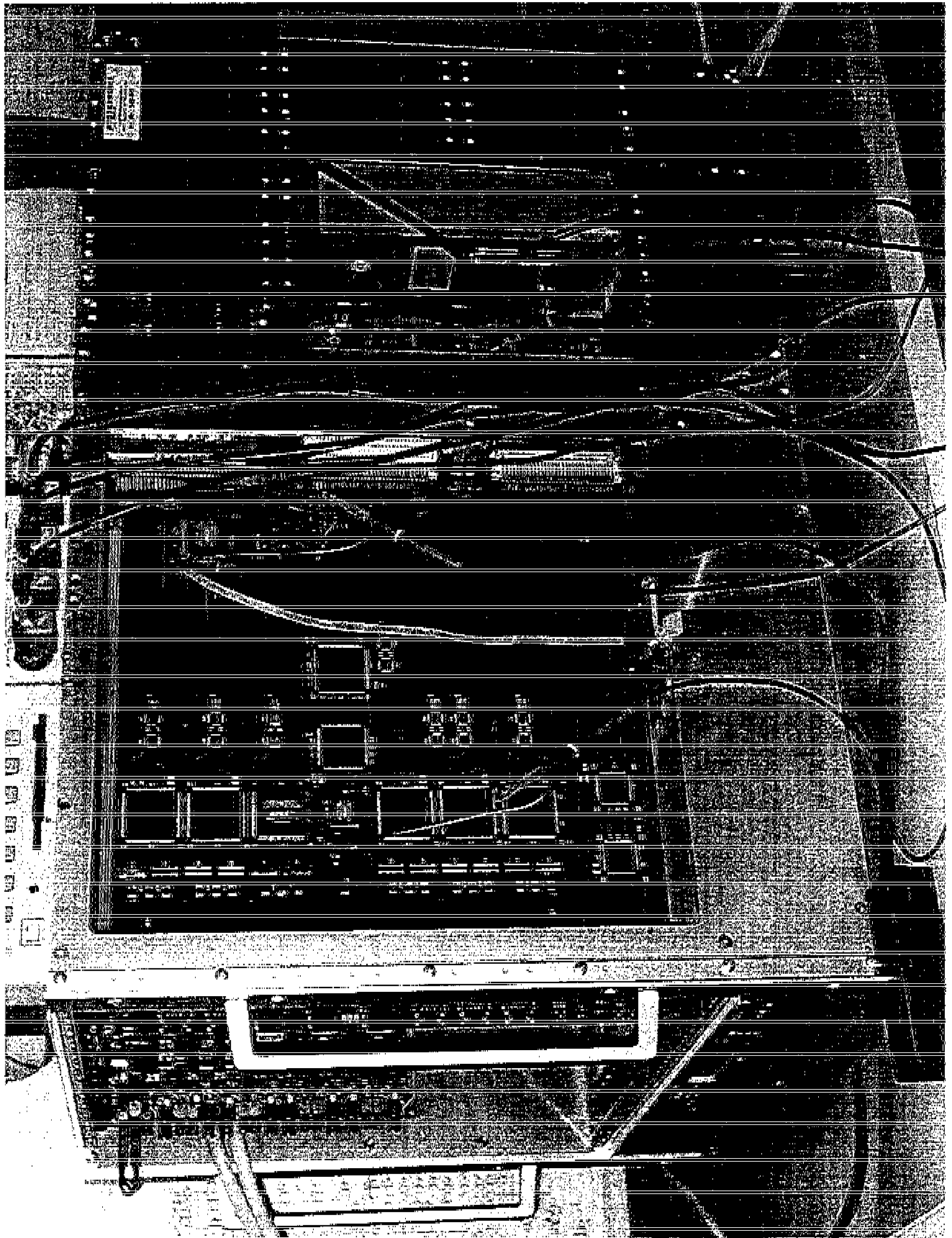
For L1.5 signals from and to...

signals for the PCI data bridge



for Lo signals from and to the neighbour module left and right

Fig.9



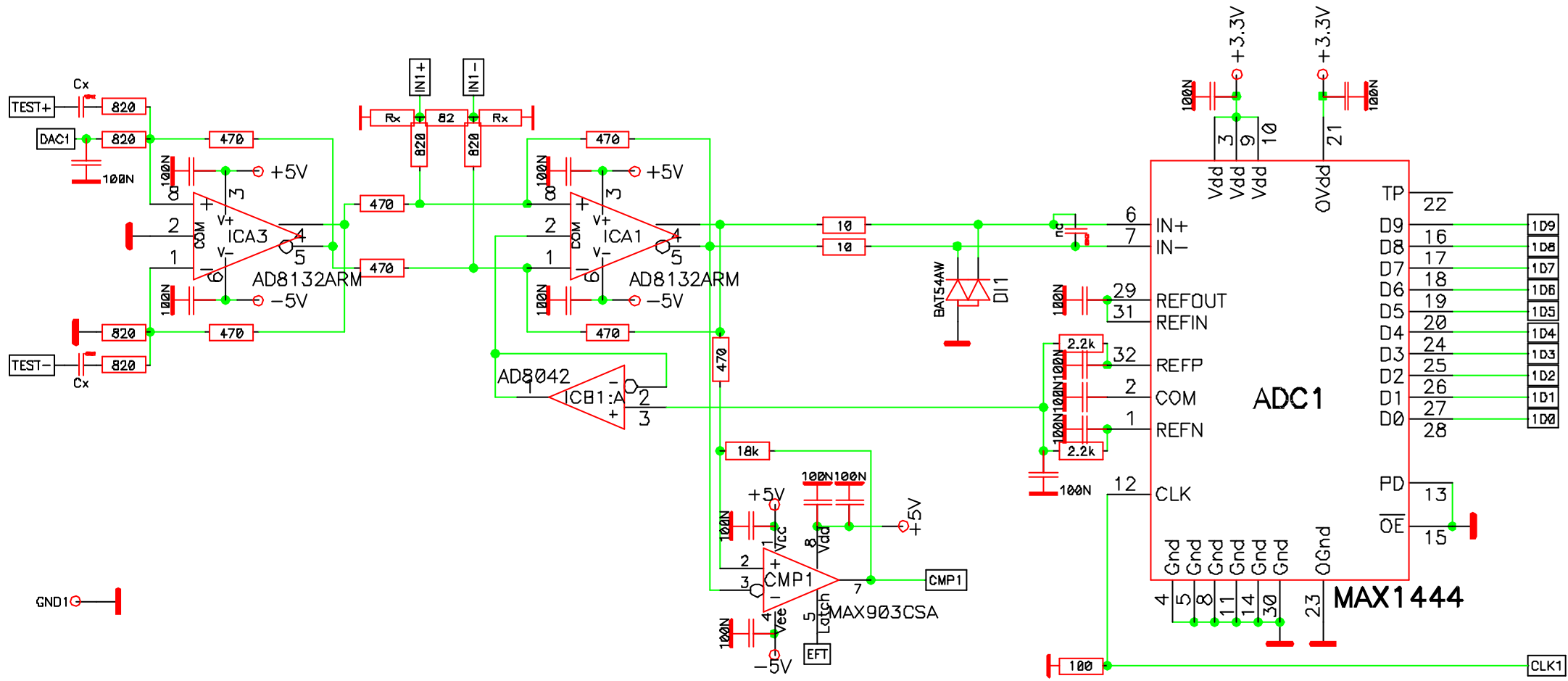


Fig.2