

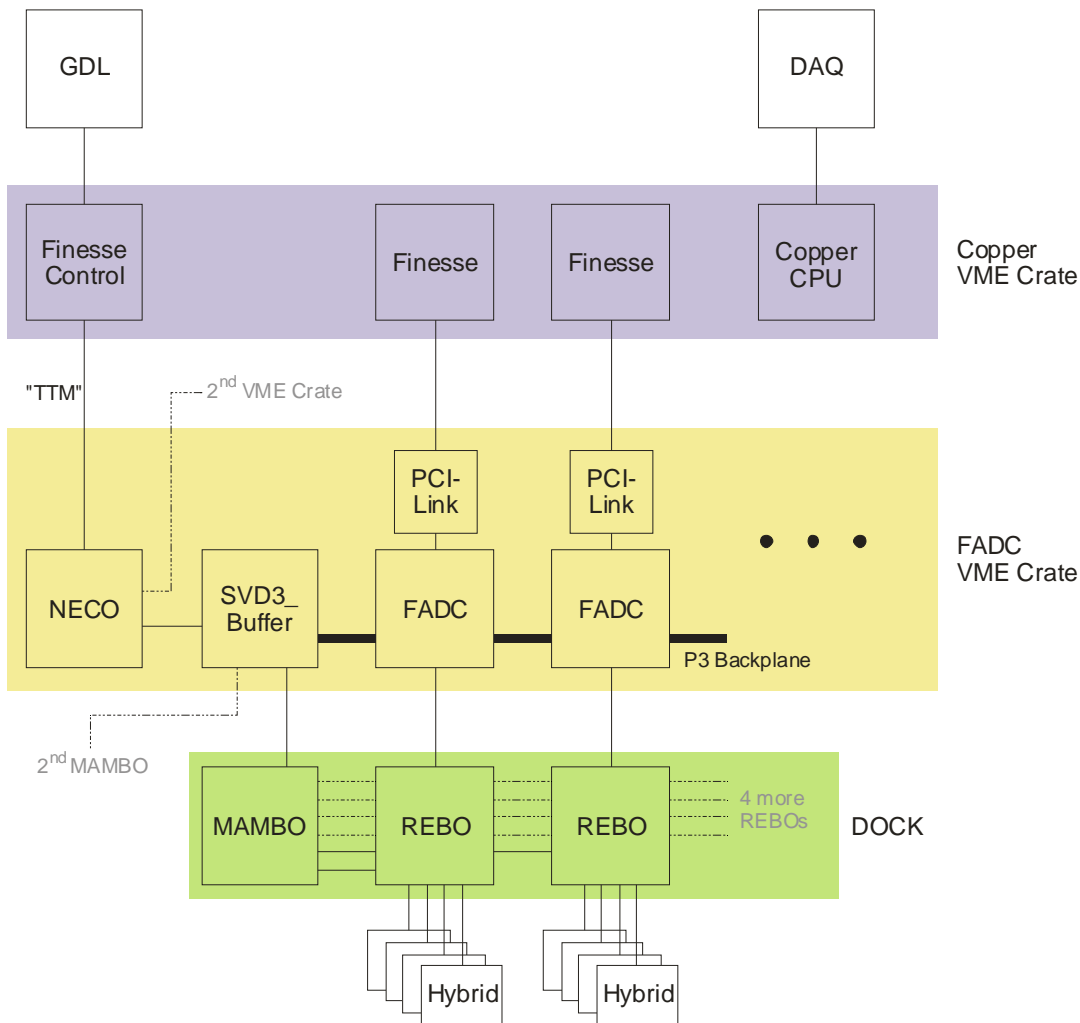
## DAQ Scheme and Beam Test Results

H. Asano, M. Friedl, H. Hyun, T. Higuchi, C. Irmeler,  
Z. Natkaniec, W. Ostrowicz, M. Pernicka, T. Tsubuyama

## Contents

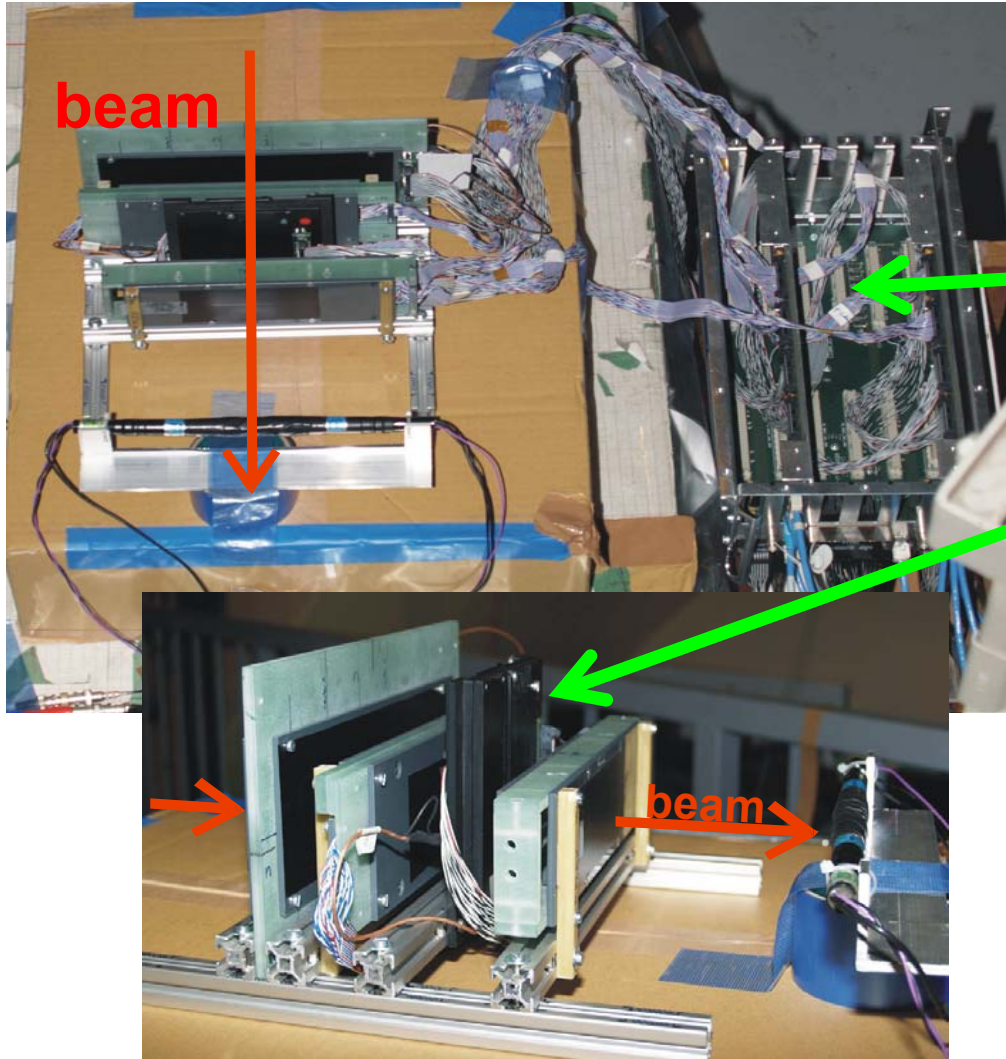
- DAQ Scheme
- Beam Test Setup
- Measurements Overview
- Beam Test Results
  - FADC system standalone
  - FADC + FINESSE + COPPER
- Summary

## Super Belle SVD DAQ Scheme



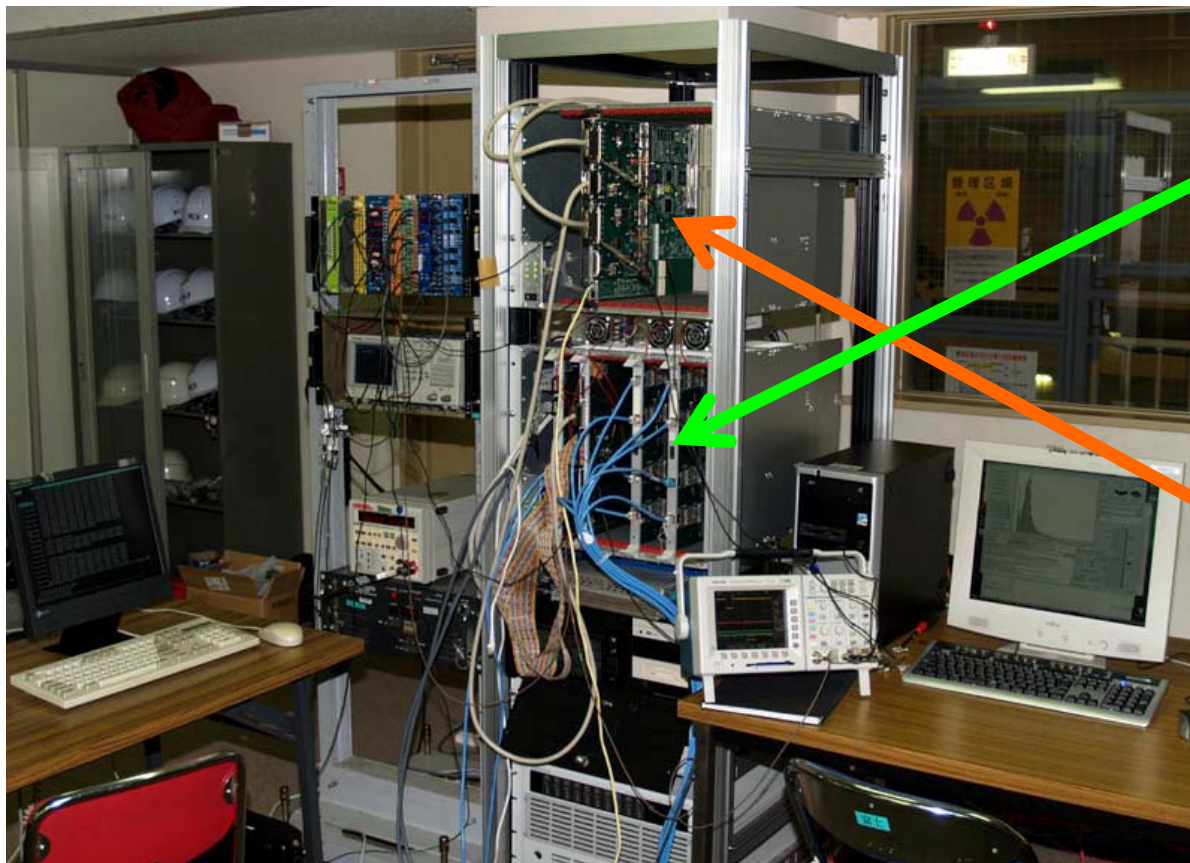
- Designed for SVD3 Upgrade
- Hybrid: 4 APV25 chips
- Dock
  - 1 Mambo
  - 2 x 3 Rebo (p- and n-side)
- FADC VME Crate
  - 1 Neco
  - 1 Buffer for 2 Dock
  - 12 FADC
- Copper VME Crate
  - 2 Finesse on each Copper
- Prototypes of FADC system exist and were already tested in several beam tests
- Whole DAQ chain was tested in current beam test.
- However: SVD4 will be ~10 times bigger

## Beam Test Setup - Frontend



- **Beam:**
  - 2 and 3 GeV  $e^-$
  - $\sim 1$  Hz trigger rate
- **Dock:**
  - 1 Mambo
  - 2 Rebo
- **Modules:**
  - JP Module
  - Micron Module
  - UV Module
  - Flex Module
- **Trigger:**
  - Scintillator
- **30 APV25 in total**

## Beam Test Setup - Backend



- **FADC system:**
  - 1 x Neco
  - 1 x Buffer
  - 2 x FADC
  - APVDAQ PC for control and VME readout
- **Copper / Finesse:**
  - 1 x Copper
  - 2 x Finesse
  - DAQ PC
- Kennwood powersupply
- Some trigger-logic



Many thanks to Higuchi-san for preparing the DAQ PC and the Copper readout software.

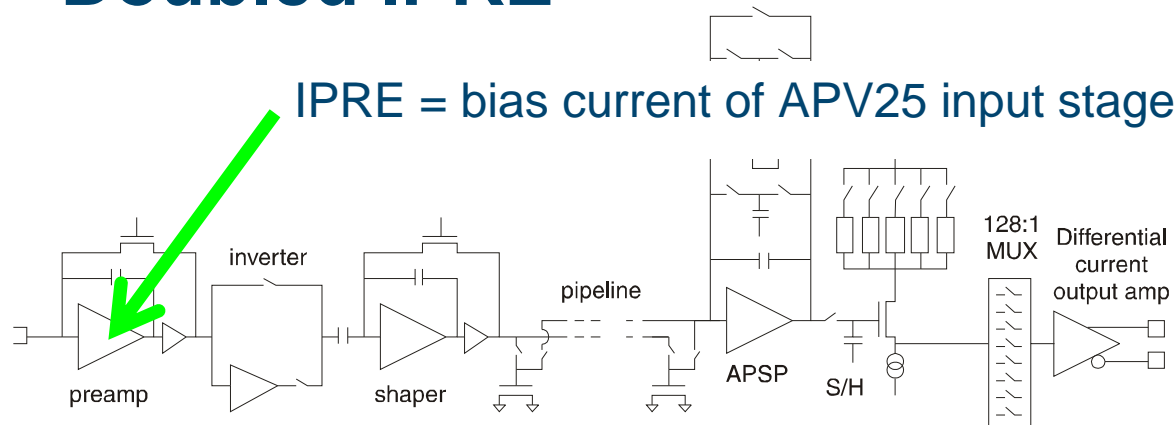


## Beam Test - Measurements

- **FADC system standalone (VME readout):**
  - Nominal APV25 settings, 40 MHz,  $T_p = 50$  ns (reference run)
  - Higher preamplifier bias current (IPRE) of the APV25 to study SNR and power consumption
  - 31.8 MHz clock frequency
- **Full DAQ system (FADC + Finesse + Copper):**
  - First time that FADC and Finesse / Copper was used together
  - Verify the interface between FADC and Finesse (clock, trigger, handshaking, event number, CRC)
  - Readout via Copper-DAQ and VME in parallel to compare data
  - Speed test

## Doubled IPRE

- **Idea:**
  - higher IPRE
  - higher gain
  - better SNR
- but also more power dissipation



- **Measurements with doubled IPRE:**
  - after switching on:
    - ~10% lower noise (and thus better SNR)
    - ~40% more power consumption @ 1.25 V plane
  - after running several hours (modules are not cooled):
    - warm up
    - same noise level as before, benefit was eaten by higher temperature
  - further measurements with proper cooling are necessary
  - we plan to do this with our Origami module next year

## Operation with 31.8 MHz clock

- **Max. L1 Trigger latency allowed by APV25:**
  - 3.8  $\mu\text{s}$  @ 42.3 MHz
  - 5.0  $\mu\text{s}$  @ 31.8 MHz preferred by **Iwasaki-san** (see talk by M. Friedl)
- **Before, we never operated APV25 with a clock lower than 40 MHz**
- **Standalone run of FADC system at 31.8 MHz**
  - worked fine
  - proper signals
  - same SNR observed
- **We also operated the FADC system with 31.8 MHz together with Copper / Finesse (modified firmware) at 42.3 MHz**
  - no problems observed
  - data are consistent

**Preliminary**

## Signal, SNR, Time-Resolution

CERN SPS June 2008: standard settings,  $T_p = 50$  ns, 40 MHz

| 120 GeV/c $\pi^+$     | Micron      |             | JP single   |             | UV          |             | Flex        |             |
|-----------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
|                       | p-side      | n-side      | p-side      | n-side      | p-side      | n-side      | p-side      | n-side      |
| Average cluster width | 1.67        | 1.13        | 2.31        | 1.92        | 2.21        | 1.88        | 2.28        | 1.91        |
| <b>Cluster SNR</b>    | <b>12.6</b> | <b>15.1</b> | <b>12.7</b> | <b>13.9</b> | <b>23.6</b> | <b>24.0</b> | <b>13.8</b> | <b>18.4</b> |
| Time resolution [ns]  | 3.91        | 3.07        | 3.51        | 2.77        | 2.58        | 1.23        | 3.52        | 1.95        |

KEK Fuji Nov. 2008: standard settings,  $T_p = 50$  ns, 40 MHz

|                       | Micron      |             | JP single   |             | UV          |             | Flex        |             |
|-----------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
|                       | p-side      | n-side      | p-side      | n-side      | p-side      | n-side      | p-side      | n-side      |
| Average cluster width | 1.77        | 1.15        | 2.34        | 1.83        | 2.36        | 1.91        | 2.34        | 1.89        |
| <b>Cluster SNR</b>    | <b>12.6</b> | <b>14.9</b> | <b>12.9</b> | <b>14.5</b> | <b>22.1</b> | <b>22.7</b> | <b>12.8</b> | <b>17.9</b> |
| Time resolution [ns]  | 3.88        | 3.07        | 3.51        | 2.73        | 2.49        | 1.39        | 3.77        | 2.02        |

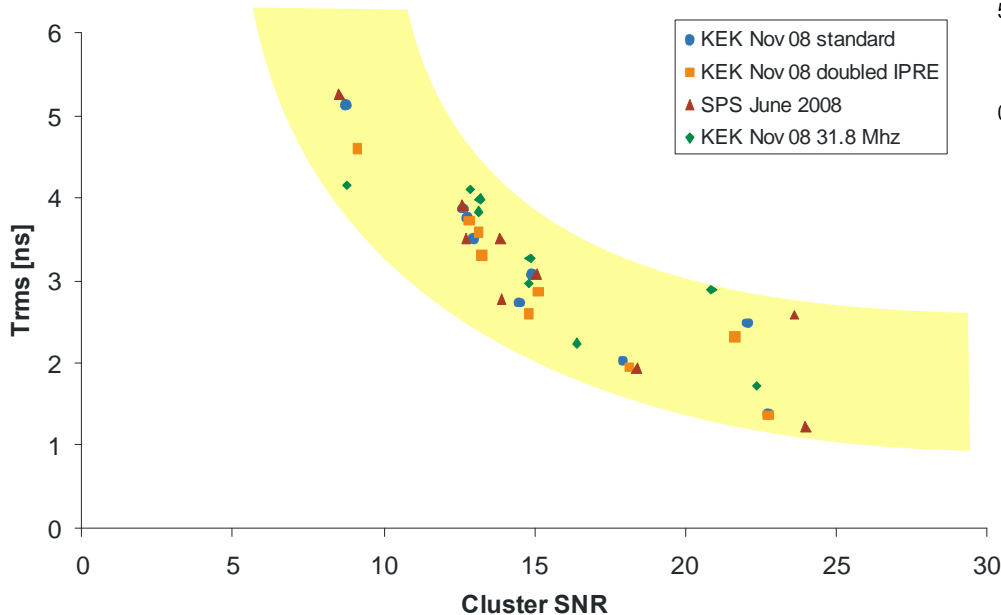
We got almost identical results for both „doubled IPRE“ and „31.8 MHz“ runs, respectively.

**Preliminary**

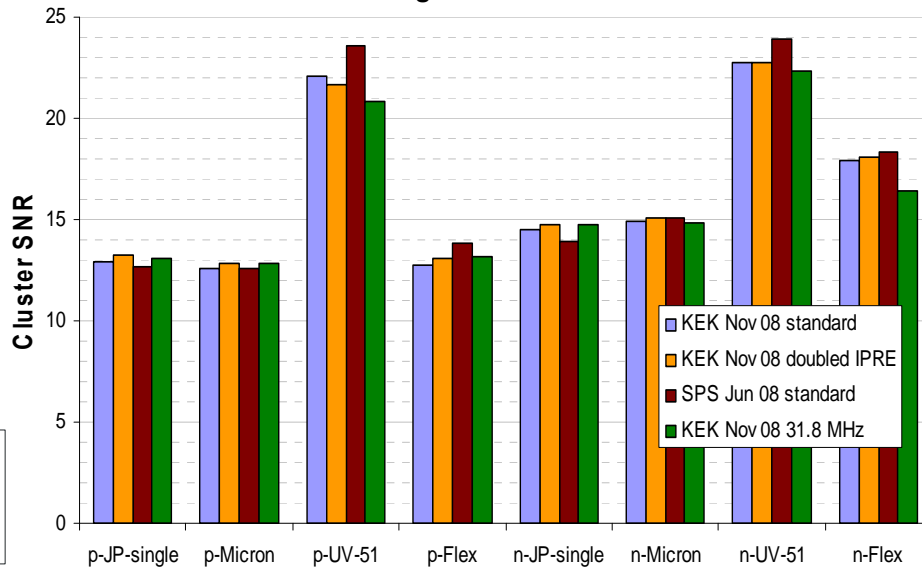
## Signal, SNR, Time-Resolution

- Values of all measurements and modules show a common trend
- Time-Resolution decreases with SNR

Peak time precision vs. SNR



Signal-to-Noise-Ratio



- SNR is almost identical in all cases
- further IPRE studies with cooling
- proper operation @ 31.8 MHz

## FADC – Finesse/Copper Tests

1. Operate FADC with clock and trigger propagated by Finesse
  - worked w/o problems → ok
2. Data transfer from FADC to Finesse
  - Finesse got data → ok
3. Readout of data via Finesse/Copper and VME in parallel and comparison
  - data match
  - few minor issues (now solved)
4. Test and verify the interface (dataflow) between FADC and Finesse
  - few issues concerning control lines (now largely solved)
5. Speed test

## FADC – Finesse/Copper – Data Issues

- **Event Number (EN):**
  - Finesse only delivered LSB → **solved**
  - Offset of 1 between Finesse and FADC
  - Finesse increments EN two clocks after trigger
    - NECO reads it too late
    - **needs Firmware modification, but solvable**
- **Checksum (CRC):**
  - Transferred at different location as expected from Finesse → **solved**
  - Values did not match → **solved**

## FADC – Finesse/Copper – Dataflow Control

- ADC-BUSY
  - was not implemented by FADC
  - Firmware modified → **solved**
- FINESSE-BUSY → **works**
- ADC-ERR and ADC-RES
  - are not implemented yet
  - behavior has to be defined
- all other control lines are working well

## FADC – Finesse/Copper Speed Test (1)

- Performed with real sparsified APV data (6 samples per event)
- Triggers from frequency generator (as beam rate is way too low)
- Noise occupancy adjustable by hit threshold of sparsification
- Copper CPU collects data and discards it (data are not stored)
  
- **Test (1): Low occupancy (0.23%)**
- 149 words / event at average (of which 96 words are overhead)
- **No problem up to 50 kHz sustained trigger rate** (APV25 limit) with Copper CPU collecting and discarding data
  - Transfer to external PC and writing to disk is limited to 5 kHz
- 50 kHz triggers correspond to 7.4 MWords/s (32 bit wide)
- **20 M events collected without any error**

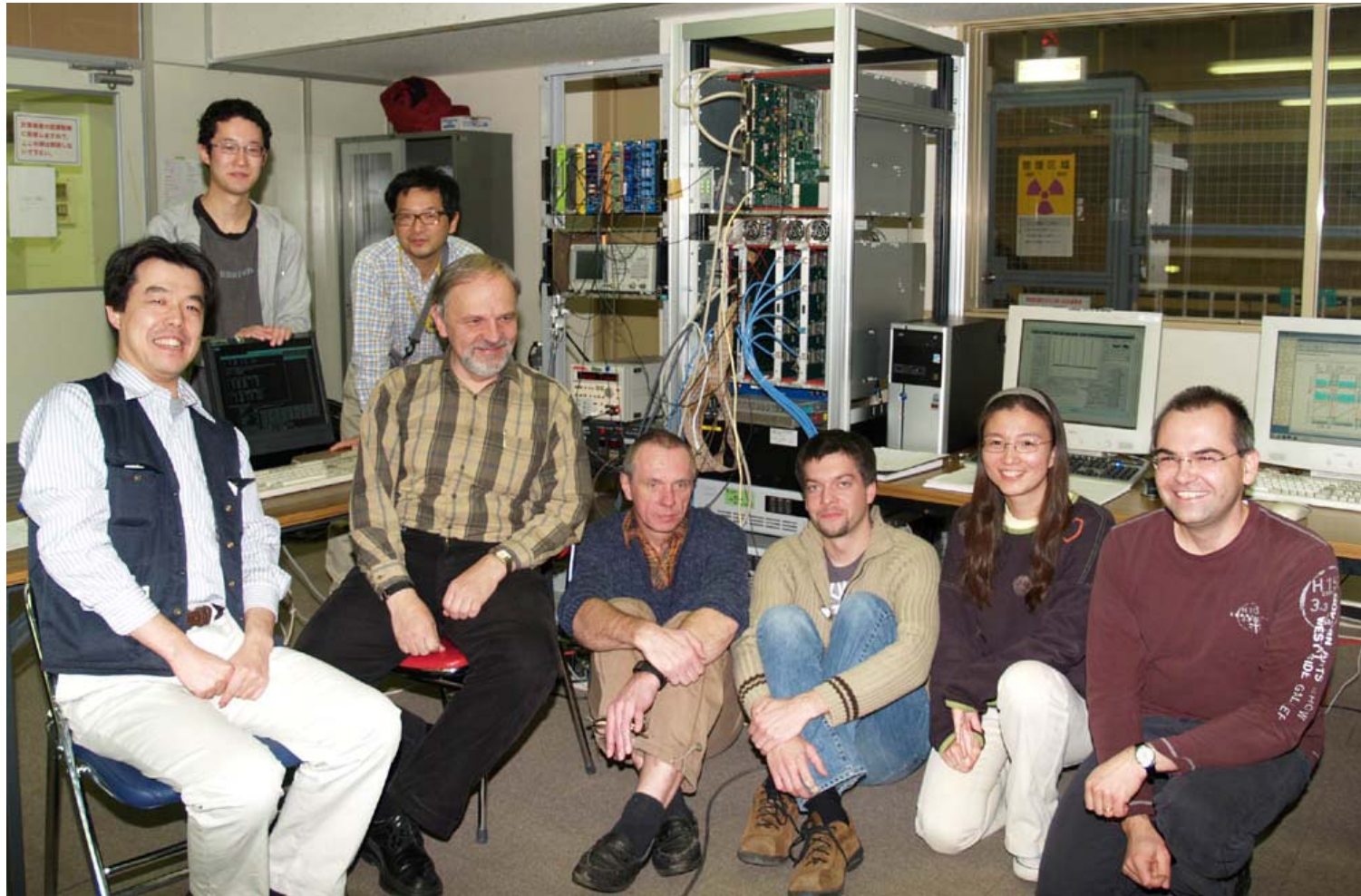
## FADC – Finesse/Copper Speed Test (2)

- **Test (2): High occupancy (24.2%)**
- 5670 words / event at average
- Works fine up to 6 kHz sustained trigger rate with Copper CPU collecting and discarding data
- Corresponding to 34 MWords/s (32 bit wide)
  - This is apparently the limit of the PCI bus (42.3 MHz frequency)
  - Deadlock observed in this (extreme) test above 6 kHz trigger rate (to be investigated)
- **Prediction for „normal“ occupancy (10%)**
- Max. trigger rate ~14 kHz
- All the above is for sending 6 APV samples/event
- Hit time finding reduces data by factor of (almost) 6 → OK for 10% occ.
- Implementation of hit finding in FPGA is underway → see talk by M.P.

## Summary

- **Beam test successfully performed at Fuji beamline**
- **Doubled IPRE of APV25:**
  - ~40% higher power disipation
  - SNR depends on temperature → needs test with cooling
- **Operating APV25 at 31.2 MHz → ok**
- **Test of DAQ chain (FADC + Finesse/Copper)**
  - works well
  - some issues concerning data and dataflow cotrol → mostly solved
- **Speed tests:**
  - Low occupancy: 50 kHz triggers w/o problems
  - High occ.: no problems up to 6 kHz trigger rate, limited by PCI bus
  - Prediction for 10% occ.: ~14 kHz possible (w/o hit time finding)
  - Higher rates (up to 50 kHz) accessible with hit time finding

## Beam Test Participants

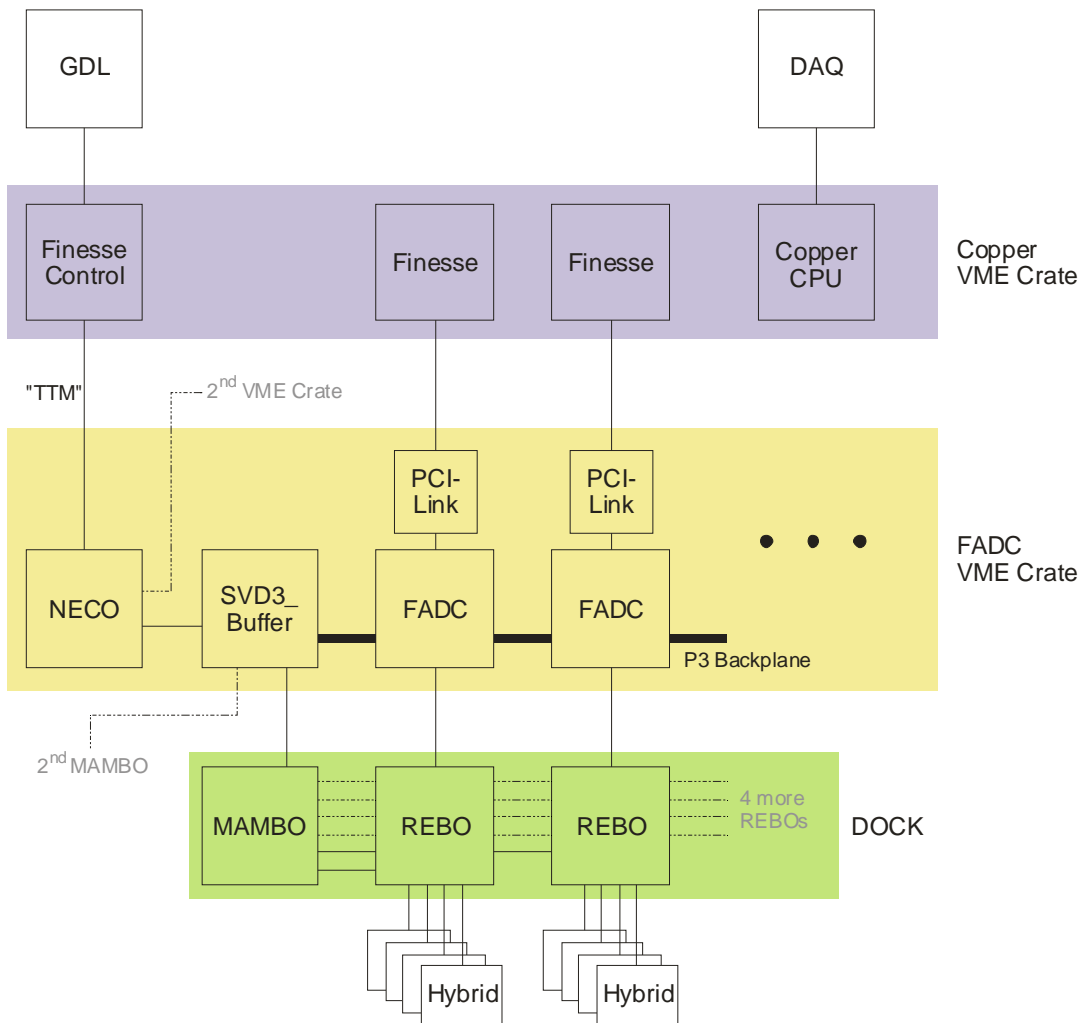




**Thank You**

# BACKUP SLIDES

## Super Belle SVD DAQ Scheme



- Designed for SVD3 Upgrade
- 384 APVs
  - 4 DOCKs
  - 4 Kenwood PSs
  - 24 FADCs
  - 2 FADC crates + 1 Copper crate
- Prototypes of FADC system exist and were already tested in several beam tests
- Whole DAQ chain (FADC & Finesse & Copper) was tested in current beam test at Fuji beam line.
- However: SVD4 will be ~10 times bigger

## Results – Signal and SNR

**Preliminary**

KEK Fuji Nov. 2008: doubled IPRE, after warming

|                       | Micron      |             | JP single   |             | UV          |             | Flex         |             |
|-----------------------|-------------|-------------|-------------|-------------|-------------|-------------|--------------|-------------|
|                       | p-side      | n-side      | p-side      | n-side      | p-side      | n-side      | p-side       | n-side      |
| Average cluster width | 1.75        | 1.15        | 2.34        | 1.85        | 2.37        | 1.93        | 2.33         | 1.88        |
| <b>Cluster SNR</b>    | <b>12.8</b> | <b>15.1</b> | <b>13.2</b> | <b>14.8</b> | <b>21.6</b> | <b>22.7</b> | <b>13.11</b> | <b>18.1</b> |
| Time resolution [ns]  | 3.72        | 2.86        | 3.30        | 2.60        | 2.31        | 1.37        | 3.59         | 1.96        |

KEK Fuji Nov. 2008: clock = 31.8 MHz

|                       | Micron      |             | JP single   |             | UV          |             | Flex        |             |
|-----------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
|                       | p-side      | n-side      | p-side      | n-side      | p-side      | n-side      | p-side      | n-side      |
| Average cluster width | 1.75        | 1.13        | 2.24        | 1.81        | 2.21        | 1.86        | 2.29        | 1.84        |
| <b>Cluster SNR</b>    | <b>12.9</b> | <b>14.9</b> | <b>13.1</b> | <b>14.8</b> | <b>20.8</b> | <b>22.4</b> | <b>13.2</b> | <b>16.4</b> |
| Time resolution [ns]  | 4.10        | 3.27        | 3.84        | 2.97        | 2.89        | 1.73        | 3.98        | 2.23        |

## Comparison VA1TA – APV25

### VA1TA (Belle SVD2)

- Commercial product (IDEAS)
- $T_p = 800\text{ns}$  (300 ns – 1000 ns)
- no pipeline
- $<10\text{ MHz}$  readout
- 20 Mrad radiation tolerance
- noise:  $ENC = 180\text{ e} + 7.5\text{ e/pF}$
- time over threshold:  $\sim 2000\text{ ns}$
- single sample per trigger

### APV25 (SuperBelle)

- Developed for CMS by IC London and RAL
- $T_p = 50\text{ ns}$  (30 ns – 200 ns)
- 192 cells analog pipeline
- 40 MHz readout
- $>100\text{ Mrad}$  radiation tolerance
- noise:  $ENC = 250\text{ e} + 36\text{ e/pF}$
- time over threshold:  $\sim 160\text{ ns}$
- multiple samples per trigger possible (Multi-Peak-Mode)

## Shaping Time and Occupancy

