ROP sends ==> RESET_DCM_xxx to reset DCM on all chips to resynchronize to the 40 MHz CLOCK signal

ROP sends ==> RESET_xxx to apply GSR onto the STARTUP module inside the FPGA therefore resetting all registers to their initial status.

ROP sends ==> V_NPROG_xxx to reconfigure all FPGAs except ROP from PROM (default)

NSYSRES goes to all FPGAs (except VME64) ==> to reconfigure all FPGAs from PROMs

PULL-UP RESISTORS apply status='11' if a CHIP has not been configured yet.
WEST MIS_095 connector

Default: Apply 3.3V to VCCO_123 (=Banks 1,2,3)

MEZZ957 TEMPLATE for 9U BOARDS
By default, HSWAP_EN is tied High (internal pull-up resistor), which shuts off pull-up resistors on the user I/O pins during configuration. When HSWAP_EN is tied Low, the pull-up resistors are on and therefore, the user I/Os have pull-up resistors during configuration.

CHECK on SHEET1: VCCO_0= LV1V5_M
CHECK on SHEET2: VCCO_123 =LV3V3 and VCCO_67=LV1V5_M

because Banks 0, 6,7 receive GTLp signals.
Default: Apply 3.3V to VCCO_123 (=Banks 1,2,3)

FRPCMU_AU58
FRPCMU_AU59
FRPCMU_AU62
FRPCMU_AU61
FRPCMU_AU19
FRPCMU_AU22
FRPCMU_AU24 FRPCMU_AU26
FRPCMU_AU48
FRPCMU_AU37
FRPCMU_AU47
FRPCMU_AU42
CSCMU_AU100
FRPCMU_AU5
FRPCMU_AU7
CSCMU_AU40
CSCMU_AU34
CSCMU_AU39
CSCMU_AU51
CSCMU_AU69
CSCMU_AU50
CSCMU_AU73
CSCMU_AU84
CSCMU_AU86
CSCMU_AU78
CSCMU_AU85

M4
M7
U1
L8

MEZZ957 TEMPLATE for 9U BOARDS

MEZZ957 TEMPLATE for 9U BOARDS

MEZZ957 TEMPLATE

HEPHY VIENNA ELEKTRONIK 1

modified by: AT 13.2.04
6-28-2004 17:34
checked by: CHECKER
0-00-0000 00:00
By default, HSWAP_EN is tied high (internal pull-up resistor), which shuts off pull-up resistors on the user I/O pins during configuration. When HSWAP_EN is tied low, the pull-up resistors are on and therefore, the user I/Os have pull-up resistors during configuration.

CHECK on SHEET1: VCCO_0 = LV1V5_M
CHECK on SHEET2: VCCO_123 = LV3V3 and VCCO_67 = LV1V5_M

because Banks 0, 6, 7 receive GTLp signals.
Place both 74LVCH16245A close to each other

LV3V3

100NF

LV3V3

Place Serial Term. Resistors close to 74LVCH16245A

Delay of L1A, BCRES from TIM to FPGA without nets on boards:

TIM: LVDS387 driver: 1- 2.9ns TIM chip: CLK input to out: 2.8 ns
GMT: LVCH16245A: 1-4 ns
Virtex2: t-setup 1.9 ns

Stand-alone Test (GMT+PSB): connect diff CLOCK via a twisted pair to a PSB board

CLK2PSB2NTP200
CLK2PSB3P
CLK2PSB4P
CLK2PSB5P
CLK2PSB6P
testpoints (+ GND) for internal CLOCK signals close to receiving chips.
FPGAs (excluding ROP) = SLAVES
FPGAs (incl. ROP) = MASTER

1. The XC18V00 accommodates serial and parallel methods of configuration. The configuration modes are selectable through a user control register in the Xilinx JTAG Programmer software. The User interface is accessible accessible through JTAG, and is set using the "Parallel mode" setting on the Xilinx JTAG Programmer software. Serial output is the default programming mode.

2. Check the CHIP schematic to find:
   - DIO8
   - PROG_AUF1
   - PROG_AUF[4:0]

3. Nets go to Mezzanine board

4. NSYSRES[6:0]

5. AUF chip

6. SWITCH BETWEEN PROM - OR VME- PROGRAMMING

7. PROG_AUF[4:0]

8. PROG_AUF

9. PROG_AUF2

10. PROG_AUF3

11. PROG_AUF4

12. Nets go to Mezzanine board

13. NSYSRES

14. NPROG jumpers: connected to /CF of Proms ...to start reconfiguration by JTAG command (all FPGAs)

15. NPROG jumpers: connected to V_NPROG_xxx...to start reconfiguration by VME command (using ROP)

16. NSYSRES7...0...to start reconfiguration after 'CRATE RESET'

17. JTAG pins: See JTAG circuits

18. By default, HSWAP_EN is tied High (internal pull-up resistor), which shuts off pull-up resistors on the user I/O pins during configuration. When HSWAP_EN is tied Low, the pull-up resistors are on and therefore, the user I/Os have pull-up resistors during configuration.

19. A persist option is available, which can be used to force configuration pins to retain their configuration
Selecting Configuration Modes

The XC18V00 accommodates serial and parallel methods of configuration. The configuration modes are selectable through a user control register in the XC18V00 device. This control register is accessible through JTAG, and is set using the “Parallel mode” setting on the Xilinx JTAG Programmer software. Serial output is the default programming mode.
Selecting Configuration Modes

The XC18V00 accommodates serial and parallel methods of configuration. The configuration modes are selectable through a user control register in the XC18V00 device. This control register is accessible through JTAG, and is set using the "Parallel mode" setting on the Xilinx JTAG Programmer software. Serial output is the default programming mode.

**JTAG pins:** See JTAG circuits
Selecting Configuration Modes

The XC18V00 accommodates serial and parallel methods of configuration. The configuration modes are selectable through a user control register in the XC18V00 device. This control register is accessible through JTAG, and is set using the “Parallel mode” setting on the Xilinx JTAG Programmer software. Serial output is the default programming mode.
Selecting Configuration Modes

The XC18V00 accommodates serial and parallel methods of configuration. The configuration modes are selectable through a user control register in the XC18V00 device. This control register is accessible through JTAG, and is set using the "Parallel mode" setting on the Xilinx JTAG Programmer software. Serial output is the default programming mode.

See CHIP schematic for JTAG circuits:

See CHIP schematic for fSRT:
HWSWAP_EN_xxx
NPWRDWN_B
DOUT_xxx

On Mezzanine boards you fSRT: M0, M1, M2
WEST MIS_095 connector

MP,270404 sheet 32

APPLY always 3.3V to all VCCO Banks

MEZZ896 TEMPLATE for 9U BOARDS

modified by: MP,270404  6-28-2004 17:32
checked by: CHECKER
By default, HSWAP_EN is tied High (internal pull-up resistor), which shuts off pull-up resistors on the user I/O pins during configuration. When HSWAP_EN is tied Low, the pull-up resistors are on and therefore, the user I/Os have pull-up resistors during configuration.
MEZZ896 TEMPLATE

MEZZ896 TEMPLATE for 9U BOARDS

APPLY always 3.3V to all VCCO Banks
By default, `HSWAP_EN` is tied High (internal pull-up resistor), which shuts off pull-up resistors on the user I/O pins during configuration. When `HSWAP_EN` is tied Low, the pull-up resistors are on and therefore, the user I/Os have pull-up resistors during configuration.
By default, HSWAP_EN is tied High (internal pull-up resistor), which shuts off pull-up resistors on the user I/O pins during configuration. When HSWAP_EN is tied Low, the pull-up resistors are on and therefore, the user I/Os have pull-up resistors during configuration.
### NORD MIS_076 connector

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PW4_1</td>
</tr>
<tr>
<td>2</td>
<td>PW4_2</td>
</tr>
<tr>
<td>3</td>
<td>PW4_3</td>
</tr>
<tr>
<td>4</td>
<td>PW4_4</td>
</tr>
<tr>
<td>5</td>
<td>PW4_5</td>
</tr>
</tbody>
</table>

### SOUTH MIS_076 connector

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PW6_1</td>
</tr>
<tr>
<td>2</td>
<td>PW6_2</td>
</tr>
<tr>
<td>3</td>
<td>PW6_3</td>
</tr>
<tr>
<td>4</td>
<td>PW6_4</td>
</tr>
</tbody>
</table>

### MEZZ10

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PW5_1</td>
</tr>
<tr>
<td>2</td>
<td>PW5_2</td>
</tr>
<tr>
<td>3</td>
<td>PW5_3</td>
</tr>
<tr>
<td>4</td>
<td>PW5_4</td>
</tr>
</tbody>
</table>

### MEZZ896 TEMPLATE for 9U BOARD

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PW5_1</td>
</tr>
<tr>
<td>2</td>
<td>PW5_2</td>
</tr>
<tr>
<td>3</td>
<td>PW5_3</td>
</tr>
<tr>
<td>4</td>
<td>PW5_4</td>
</tr>
</tbody>
</table>

**APPLY always 3.3V to all VCCO Banks**
WEST MIS_095 connector

APPLY always 3.3V to all VCCO Banks

MEZZ896 TEMPLATE for 9U BOARDS
By default, HSWAP_EN is tied High (internal pull-up resistor), which shuts off pull-up resistors on the user I/O pins during configuration. When HSWAP_EN is tied Low, the pull-up resistors are on and therefore, the user I/Os have pull-up resistors during configuration.
JTAG: Xilinx Config. options: VME, Par_CableIV, Bridge-backplane
JTAG: Altera Config. options: VME, Master Blaster, Bridge-backplane

XILINX chips configured also directly by VME.

Choose Configuration mode: default = VME

Select Configuration mode: default = VME

74LVCH16245 protects progr.chips against +5V.

To remove PROM or FPGA from chain:
1) Disconnect TMS => internal R-pullup keeps TAP controller in RESET status
2) Remove TDO of Prom/FPGA from TDI-TDO chain.

10k to 1-2 (LV3V3=>TRST) or 0R to 2.3 (GND=>TRST)

MASTER BLASTER
Run MasterBlaster either with 3.3 or 5V

Select Configuration mode: default = VME

ELEKTRONIK 1
The Virtex chips are mounted on mezzanine boards.

 ===> There is no JTAG hetero symbol for Virtex chips.
MEZZ957 TEMPLATE for 9U BOARDS

WEST MIS_095 connector

EAST MIS_095 connector

Default: Apply 3.3V to VCCO_67 (=Banks 6,7) for GTL+ signals

Default: Apply 3.3V to VCCO_123 (=Banks 1,2,3)
By default, HSWAP_EN is tied High (internal pull-up resistor), which shuts off pull-up resistors on the user I/O pins during configuration. When HSWAP_EN is tied Low, the pull-up resistors are on and therefore, the user I/Os have pull-up resistors during configuration.

CHECK on SHEET1: VCCO_0 = LV3V3
CHECK on SHEET2: VCCO_123 =LV3V3 and VCCO_67=LV3V3
only LVTTL signals to/from LFF chip
By default, HSWAP_EN is tied High (internal pull-up resistor), which shuts off pull-up resistors on the user I/O pins during configuration. When HSWAP_EN is tied Low, the pull-up resistors are on and therefore, the user I/Os have pull-up resistors during configuration.

CHECK on SHEET1: VCCO_0= LV3V3
CHECK on SHEET2: VCCO_123 =LV3V3 and VCCO_67=LV3V3
only LVTTL signals to/from LFF chip
By default, HSWAP_EN is tied Low (internal pull-up resistor), which shuts off pull-up resistors on the user I/O pins during configuration. When HSWAP_EN is tied Low, the pull-up resistors are off and therefore, the user I/Os have pull-up resistors during configuration.

CHECK on SHEET1: VCCO_0= LV3V3
CHECK on SHEET2: VCCO_0= LV3V3, VCCO_123 =LV3V3 and VCCO_67=LV3V3
MEZZ957 TEMPLATE

MEZZ957 TEMPLATE for 9U BOARDS

Default: Apply 3.3V to VCCO_123 (=Banks 1,2,3)

Default: Apply 3.3V to VCCO_67 (=Banks 6,7)

AUB,AUF SRT: Apply 1.5V to VCCO 67 (=Banks 6&7) for GTL+ signals

MEZZ957 TEMPLATE

SRT

HEPHY VIENNA
ELEKTRONIK

modified by: AT 13.2.04
6-28-2004 17:34

checked by: CHECKER
0-00-0000 00-00-00
By default, HSWAP_EN is tied High (internal pull-up resistor), which shuts off pull-up resistors on the user I/O pins during configuration. When HSWAP_EN is tied Low, the pull-up resistors are on and therefore, the user I/Os have pull-up resistors during configuration.

CHECK on SHEET1: VCCO_0= LV3V3
CHECK on SHEET2: VCCO_123 =LV3V3 and VCCO_67=LV1V5_M

because Banks 6,7 receive GTLp signals.
CS5206 Linear 6A Voltage Regulator

1.5V for INF, AUF, INC, LFF, ROP chips

CS5206 Linear 6A Voltage Regulator

1.5V for IND, LFB, INB, AUB, SRT chips

V_{\text{ref}}
\begin{align*}
(1.240...1.254).V/68.1 & = 18.2...18.6 \text{ mA} > 10 \text{ mA} \\
250 \text{ mV} (18.2...18.6 \text{ mA}) & = 13.73...13.44 \text{ Ohm} \\
\text{Adjust voltage with } R_{131} & = 475...562 \text{ Ohm} \\
I_{\text{adj}} & = 54 \text{ uA}...\text{can be neglected}
\end{align*}

all resistors for CS5206 in metalfilm

100 mm Heatsink

30.7 2004: 100 mm Heatsink DECAL CHECK FEHLT NOCH !!
22 Ohm resistors protect the Virtex drivers against overvoltage spikes.

<table>
<thead>
<tr>
<th>Parity bit: for odd parity</th>
<th>GA=00001 =&gt; GAP=0</th>
<th>slot=1: GA=00001 =&gt; GAP=0</th>
<th>slot=3: GA=00011 =&gt; GAP=1</th>
</tr>
</thead>
<tbody>
<tr>
<td>in slot</td>
<td>inverted values</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Keep NDTACK NERR inactive while VME64X chip is unconfigured.

See VME64x.pdf page 10 Table 3-2

47 Ohm resistors protect the Virtex drivers against overvoltage spikes.

**GMT9U must not inserted into the 6U Backplane!!!**

Do not use LV2V5 and LV1V8 from BACKPLANE-6U.

LV2V5 and LV1V8 will not be connected on the Backplane-9U. Do not solder this part.

Unused 2.5V plane can be connected to 3.3V optionally on 9U backplane if GTL-6U is not used anymore in Crate.

**GMT9U**

**VME INTERFACE**

HEPHY VIENNA

ELEKTRONIK I

modified by: H. BERGAUER  7-27-2004 16:53

checked by: A TAUKOK  8-18-2003 16:53
First ADDRESS BUS: 19-1 to Xilinx chips
Second ADDRESS BUS: 24-1 to ROP and other chips

First ADDRESS BUS: 19-1 to Xilinx chips
Second ADDRESS BUS: 24-1 to ROP and other chips

**FRAGEN bitte klären:**

- 3.3V fehlen: 22 42 118 146... pdf falsch?? Ja, pinfile ist Referenz, HB 200807
- 2.5V fehlen: 33 48 91 130 201... pdf falsch?? Ja, pinfile ist Referenz, HB 200807
- Dedicated inputs als GND definiert: 78 80 182 184
- Unused CLK pin als GND definiert: 183
- INIT DONE used als I/O: 19
- Checked by AT 18.Aug.03

---

GMT9U
VME INTERFACE
HEPHY VIENNA
ELEKTRONIK 1
modified by: M.PADRTA 7-30-2004_10:35
checked by: CHECKER 0-00-0000_00:00

Sheet 2 of 3

Baseaddress
S31-S24 not used by VME64
S31-S24 necessary for standard VME logic

---

S1-S24 not used by VME64
S1-S24 necessary for standard VME logic
A.T. Aug03: See configdevices.pdf:
Do not insert R75, R76, R77 when internal pullup R are used in IC20: EPC2
All pull-up resistors are 1 k.

This pin is the power or ground for the ClockLock and
ClockBoost circuitry of a PLL. To ensure noise resistanc
e of the power and ground supply to the ClockLock and
ClockBoost circuitry should be isolated from the power and ground to the rest of the device. If the PLL is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.

Dedicated inputs als GND definiert:  78 80 182 184
Unused CLK pin als GND definiert:  183

INIT_DONE used as I/O: 19

Checked by AT 18.Aug 03

FRAGEN bitte klären:
3.3V fehlen: 22 42 118 146.....pdf falsch?? Ja, pinfile ist Referenz, HB 200803
2.5V fehlen: 33 48 91 130 201....pdf falsch?? Ja, pinfile ist Referenz, HB 200803
Dedicated inputs als GND definiert: 78 90 182 184

INIT_DONE used as I/O: 19

GMT9U
VME INTERFACE

HEPHY VIENNA
ELEKTRONIK 1
modified by: H. BERGAUER 7-29-2004 16:01
checked by: CHECKER 8-18-2003 15:51

sheet 3 of 3