CMS L1 Global Muon Trigger Update

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Trigger Meeting, CMS Week, CERN
4th December, 2001

Hardware status
Thoughts on halo triggers
Simulation

URL of this presentation:
CMS Level-1 Trigger

CaloTrigger
- CAL Readout
  - Regional CALO Trigger
    - GLOBAL CALORIMETER TRIGGER
      - Bristol
        - MIP & quiet bits (2x 252)
  - Wisconsin

RPC
- Pattern Comparator
  - Warsaw

PACT
- Track Correlator
  - Trigger Server

DTBX
- Bunched Track Finder
  - HEPHY Vienna

CSC
- Endcap Track Finder
  - Endcap Trigger
    - CSC Sorter
      - Strip cards
        - Motherboard

RPC Sorter
- Bari

DT Sorter
- Bologna

GLOBAL MUON TRIGGER

GLOBAL L1 TRIGGER

L1 Accept …………
max. 100 kHz

Pipe-lined
40 MHz

4+4 μ
4 μ
4 μ

HEPHY Vienna

HeoL1 Global Muon Trigger Update
Principle of the GMT

**Inputs:**
8 bit $\phi$, 6 bit $\eta$, 5 bit $p_T$, 1 bit charge, 3 bit quality

**Output:**
8 bit $\phi$, 6 bit $\eta$, 5 bit $p_T$, 1 bit charge, 3 bit quality, 1 bit MIP, 1 bit Isolation

**Further Inputs:**
MIP and Quiet Bits of 252 calorimeter regions

- Increase efficiency
- Reduce ghosts
- Reduce trigger rate by improving $p_T$ assignment
- Add MIP & ISO bits from calorimeter

Best 4 $\mu$
 GMT in the Global Trigger Crate

→ 1 GMT Logic Board (front panel 4 slots wide)
→ 3 PSB boards to receive calorimeter information
PSB 6 channel prototype

Prototype available
Hannes Sakulin  
CERN/EP  
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CERN, 4th December 2001

**GMT single-board solution**

Latency: 14 bx

**Single board Global Muon Trigger**

- Front panel
  - 4µ RPC fwd
  - 4µ CSC
  - 4µ RPC barr
  - 4µ DT
- LVDS receivers: 16 SCSI-2
- VME/ROPuat
- fwd_LOGIC FPGA
- GMT-IN FPGA: 4µ
- synchronisation, readout, ...
- ISO/MIP: 4µ
- CMS/DT: cancel out
- CSC/DT cancel out
- ISO/MIP: 4µ
- HANDLE: 4µ barr
- barrel_LOGIC FPGA
- barrel PROJECTION FPGA
- forward PROJECTION FPGA
- η converters, SINGLE
  - MATCH & PAIR LOGIC
  - η converters, SINGLE
  - MATCH & PAIR LOGIC
- MUON MERGER & fwd SORTER
- MUON MERGER & fwd SORTER
- fwd: (180MIP+180 ISO)/2
- barr: (144 MIP+144 ISO)/2
- MIP+ QUIET bit
- Reformatting
- ChLink
- LIA...
- 16 pins
- 10 pins
- 52 pins
- 80MHz GTLP
- 180 pins
- 144 pins
- 16 pins

All logic functions defined
### GMT Hardware schedule

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<td>H1</td>
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#### Milestones / Plans:

- **2001** Logic design, ORCA + VHDL Simulation
  - **Dec 2001** Logic design finished
    - Logic functions defined “up to the last bit”.
    - Chip types, bus widths, LUTs, registers, read-out processing,… defined.
- **2002** VHDL Simulation, Design of FPGA chips
  - **Dec 2002** FPGA design finished
- **2003** Production of VME 9U Boards
- **2004/05** Integration tests, production of spare boards
Progress in 2001:  
- All logic functions defined  
  - Chip Models selected (mostly Virtex II), Interconnections defined  
  - Design compacted (external RAMs moved into big FPGAs)  
  - 50-page internal GMT design document + drawings  
- Functionality improved  
  - DT/CSC cancel-out unit (improved performance in barrel/endcap overlap region)  
- Simulation studies  
  - ORCA Simulation extended and improved (calo projection, cancel-out unit, …)  
  - studies to optimize GMT design parameters and performance  

Plans for 2002:  
- continue VHDL simulation of FPGA chips  
- VHDL simulation of GMT board  
- Synthesis / design of FPGAs  
- in parallel further studies with ORCA
The situation

- halo muons are seen by CSC, only (flag indicates halo muon)
- 4 bunch crossings delay between the two endcaps
- read-out will only work correctly in one half of the detector, where halo muon is moving away from interaction point
- do we need matching between the endcaps for alignment?
Possible algorithms (from GMT point of view)

A) no matching between endcaps
   A1) Change read-out to read CSC data also from 4 bx earlier (if halo trigger)
   A2) get 2 L1 accepts within 4 bx (can interfere with other triggers)

B) Matching without direction-information
   • GMT stores all halo muons in pipeline and matches with halo muons 4 bx later
   • works if we want to trigger only on matched halo muons (both endcaps)
   • if we also want to trigger on unmatched halo muons we get double triggers

C) Matching with direction information
   • we get direction information from CSC: fromIP / toIP
   • GMT stores toIP halo muons in pipeline and matches with fromIP halo muons 4 bx later
   • can trigger on matched and/or unmatched halo muons
Monte Carlo production (Pythia 6.152, CMSIM 121)
- using Pythia default normalization
- lower $p_T$-cut (p-cut) in forward region
  (now $p > 3.5$ GeV/c, in 2000: $p_T > 1.5$ GeV/c)
- increased $\eta$-range up to in CMSIM
  (now 5.5, in 2000: 2.5)
- muons in pile-up vetoed
- LHC luminosity $L = 2 \times 10^{33}$ cm$^{-2}$s$^{-1}$
- new (Nov 2001): increased statistics

L1 Trigger simulation (ORCA 5.3.1)
- new CSC Trigger Primitives (since ORCA 5.1.2)
- updated CSC Track Finder (since ORCA 5.1.2)
- updated Global Muon Trigger (since ORCA 5.1.2)
- new with respect to last processing
  - DT re-digitized, updates in CSC Trigger and CSC Track Finder
- RPC: without noise and neutral background simulation

<table>
<thead>
<tr>
<th>Sample</th>
<th>$L_{\text{int}}$/nb$^{-1}$</th>
<th>Events in luminosity</th>
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<tr>
<td>mu_MB1mu_pt1</td>
<td>0.0247</td>
<td>231k (x1.5)</td>
</tr>
<tr>
<td>mu_MB1mu_pt4</td>
<td>0.4071</td>
<td>107k (x2)</td>
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<tr>
<td>mu_MB1mu_pt10</td>
<td>2.81</td>
<td>41k</td>
</tr>
<tr>
<td>W_1mu</td>
<td>2856.</td>
<td>43k</td>
</tr>
<tr>
<td>Z_1mu</td>
<td>2336.</td>
<td>50k</td>
</tr>
<tr>
<td>mu_MB2mu</td>
<td>0.2935</td>
<td>32k (x3)</td>
</tr>
</tbody>
</table>

background samples – 2001 muon production
Generated rates

~200 Hz in year 2000 production (scaled to L=2x10^{33})

L=2x10^{33} cm^{-2} s^{-1}
L1 single muon trigger rates
samples: pt1, pt4, pt10, W, Z

whole detector: 0 < |\( \eta \)| < 2.5

\[ L = 2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1} \]

- **50 kHz DAQ**
  - 3.5 kHz @ 14 GeV/c
  - Scaled from TDR: 7.1 kHz

- **75 kHz DAQ**
  - 5.5 kHz @ 12 GeV/c
  - Scaled from TDR: 10.6 kHz

- **25 kHz DAQ**
  - 1.55 kHz @ 20 GeV/c
  - Scaled from TDR: 2.9 kHz

**Graph Details:***
- **Y-axis**: Trigger Rate (Hz)
- **X-axis**: muon \( p_T^{\text{cut}} \) (GeV/c)
- **Legend**:
  - Gen
  - DT + CSC
  - RPC
  - GMT Sep2001 tuning
  - GMT Nov2001 tuning
Nov 2001 Re-tuning of GMT algorithm

L1 efficiency

GMT Sep2001 tune

L = 2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}

GMT Nov2001 tune

\text{eff} = 96.5 \%

\text{eff} = 96.9 \%

\eta \rightarrow \text{(*)efficiency to find muon of any } p_T \text{ in flat } p_T \text{ sample}
L1 di-muon trigger rates
samples: pt1, pt4, pt10, 2mu_pt1, GMT Nov 2001 tune

trigger rates in Hz

\( L = 2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1} \)
L1 di-muon trigger rates, $p_{T,2} \geq 4$ GeV/c
samples: $pt1$, $pt4$, $pt10$, $2mu_{pt1}$, GMT Nov 2001 tune

Di-muon Rates - $p_{T,2} \geq 4$ GeV/c

Trigger Rate / Hz

$10^3$

$10^2$

$10^1$

$10$

$L=2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$

muon $p_{T,1}^{\text{cut}}$ (GeV/c)

$4$  $6$  $8$  $10$  $12$  $14$  $16$  $18$  $20$

Gen

DT + CSC

CSC

RPC

GMT

GMT from ghosts

GMT 2 $\mu$ from 1 event

GMT 2 $\mu$ from 2 events in 1 bx

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L1 single & di-muon trigger rates
symmetric di-muon cut, GMT Nov 2001 tune

L1 single and di-muon trigger rates

trigger rates in kHz

L = 2 x 10^{33} \text{ cm}^{-2} \text{s}^{-1}

binning

L1 Global Muon Trigger Update
L1 single and di-muon trigger rates, lower di-muon cut: 3.0 GeV/c

Trigger rates in kHz

L = 2 x 10^{33} cm^{-2} s^{-1}

Lower threshold 3 GeV/c

Binning
Conclusion

- Progress in hardware design as planned
  - all logic functions defined
    - design compacted & improved
    - new solution with one logic board

- Planned R&D in 2002
  - VHDL simulation of FPGAs and board
  - design of FPGAs

- Trigger on halo muons:
  - GMT can provide matching between endcaps with delay
  - possible during normal physics running

- Simulation results with 2001 muon production
  - results with increased statistics for low luminosity scenario
  - GMT re-tuned to increase efficiency in the overlap region
  - $p_T$-cut was lower than in last year’s production
  - improved CSC trigger & GMT can cope with higher background rate