CMS Global Muon Trigger Update

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CMS Week, CERN
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Topics:
- Hardware
- Firmware
- Online Software

URL of this presentation:
CMS Level-1 Trigger

Calorimeter Trigger

- HF
- HCAL
- ECAL

Regional Calorimeter Trigger

Global Calorimeter Trigger

Muon Trigger

- RPC
- CSC
- DT

Pattern comparator trigger

CSC local trigger

CSC Track Finder

DT local trigger

DT Track Finder

Global Muon Trigger

L1 Global Trigger

4+4 μ

4 μ

4 μ

4 μ (with MIP/ISO bits)

Max. 100 kHz

L1 Accept

Pipelined 40 MHz, Latency < 3.2 μs
Global Muon Trigger Overview

252 MIP bits
252 Quiet bits
4 μ RPC brl
4 μ DT
4 μ CSC
4 μ RPC fwd

Inputs:
8 bit $\phi$, 6 bit $\eta$, 5 bit $p_T$,
2 bits charge, 3 bit quality,
1 bit halo/$\eta$ fine-coarse

Output:
8 bit $\phi$, 6 bit $\eta$, 5 bit $p_T$,
2 bits charge/synch, 3 bit quality, MIP bit, Isolation bit
Global Muon Trigger Tasks

- Synchronizing
- Matching & Pairing
  - DT & brlRPC, CSC & fwdRPC
- Merging parameters
- Converting scales ($\eta$)
- Detecting ghosts, fake triggers
- Canceling out duplicated candidates in the overlap region
- Propagating to calo/vertex for MIP/Iso bit assignment
- Ranking & Sorting
 GMT in the Global Trigger Crate

1 GMT Logic Board

FPGA firmware ready
Board in Layout stage

3 Pipeline Sync. Boards

6-channel prototype available

Special wide input board parallel to front panel

Global Trigger Crate
(top view)

4 DT/CSC + 8 RPC muons

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GMT Logic Board

Front panel

LVDS receivers

16 SCSI

4µ RPC fwd

4µ CSC

4µ DT

4µ RPC brl

GMT IN FPGA

XC2V1500 FF896

XC2V3000 BF957

Forward Logic FPGA

VME / ROP

VME Intfc

DAQ readout

JTAG, C lock

P1/P2

10 pins

80MHz GTLp

ChLink

16 pins

52 pins

180 pins

144 pins

16 pins

4 muons 26x4 bits

FINAL GMT SORTER

4µ fwd

4µ brl

FPGA

GMT IN FPGA

XC2V1500 FF896

Barrel Logic FPGA

GMT IN FPGA

XC2V1500 FF896

Barrel MIP and ISO Assignment FPGA

GMT IN FPGA

XC2V1500 FF896

Forward MIP and ISO Assignment FPGA

(Mezzanine for FF896 ready & tested, Mezzanine for BF957 produced)
GMT Logic Board: Routed Layout

Connectors to input board

4 SCSI connectors on Logic Board

3x4 on input board

LVDS receivers

Input fwdRPC

Input CSC

Input DT

Input btrRPC

Logic fwd

Logic btr

MIP/ISO fwd

MIP/ISO btr

SORT

RPC

M. Padrta
Routing between two Chips

Configuration PROMS
Under Mezzanine board

Orthogonal and diagonal routing layers used.

12 layer print

M. Padrta
Mounted in Parallel to front panel of crate.
Connectors for 2\textsuperscript{nd} 3\textsuperscript{rd} and 4\textsuperscript{th} muon
from DT, CSC, barrel RPC, forward RPC

Layout and routing finished.
Production this month.

M. Padrta
Mezzanine BF957

- For 6 chips on GMT Logic Board
  - Logic FPGAs
  - MIP/ISO Assignment FPGA
  - Sort FPGA
  - ROP
Status of GMT Logic Board

- 9U Backplane produced & tested
  - All connectors defined
- Mezzanine for FF896 package exists
  - Input FPGAs
- Mezzanine for BF957 produced and under test (16 pieces)
  - Logic, MIP/ISO Assignment, Sort FPGAs

- Schematics complete
  - M. Padrta, A. Taurok (Vienna)
- Layout & Routing complete, currently doing final checks
  - M. Padrta, A. Taurok (Vienna)
- Production planned this month
Status of GMT Firmware

- Firmware for all chips complete (10 Virtex II)
- Recently completed ROP Chip, including
  - Readout Logic
    - Collects data from input chips and Sort chip
    - Sends data on channel link to GT/GMT readout board
    - Full board has been simulated
      - channel link record verified.
  - Board Control
    - Access to reset lines
    - Access to status lines
    - Access to programming lines of the other FPGAs via VME
  - VME Controller
    - Distributes VME signal to all other chips
  - JTAG Controller to access JTAG via VME
    (using VHDL developed by J. Erö)
Readout to DAQ on GMT Logic Board

1) 512b ring buffer
1k de-randomizing FIFO

2) Parallel readout busses to ROP chip (point-to-point)

3) ROP Chip

4) Channel Link to Global Trigger Front End Card

LVDS receivers

4µ RPC fwd

4µ CSC

4µ DT

4µ RPC brl

GMT-IN FPGA 4µ

Forward MIP and ISO Assignment FPGA

Forward Logic FPGA

Barrel MIP and ISO Assignment FPGA

Barrel Logic FPGA

GMT-IN FPGA 4µ

GMT-IN FPGA 4µ

GMT-IN FPGA 4µ

GMT-IN FPGA 4µ

VME Intfc

VME

FPGA

FPGA

FPGA

512b ring buffer

1k de-randomizing FIFO

Parallel readout busses to ROP chip (point-to-point)

ROP Chip

Channel Link to Global Trigger Front End Card

16 SC512

160MHz GTLp

180 pins

144 pins

16 pins

16 pins

10 pins

144 MIP+144 ISO)/2

(180 MIP+180 ISO)/2

(144 MIP+144 ISO)/2

ROP Chip

JTAG Clock

LVDS receivers

4µ RPC fwd

4µ CSC

4µ DT

4µ RPC brl

GMT-IN FPGA 4µ

Forward MIP and ISO Assignment FPGA

Forward Logic FPGA

Barrel MIP and ISO Assignment FPGA

Barrel Logic FPGA

GMT-IN FPGA 4µ

GMT-IN FPGA 4µ

GMT-IN FPGA 4µ

GMT-IN FPGA 4µ
GMT consists of
- 3 pipeline synchronizing boards … prototype available
- 1 GMT logic board + front panel … almost complete for production board production this month

FPGA design for GMT logic board in progress
- Input FPGA (4x) … firmware completed
- MIP and ISO assignment unit (2x) … firmware completed (brl+fwd)
- GMT logic FPGA (2x) … firmware completed (brl+fwd)
- Sorter FPGA (1x) … firmware completed
- ROP Chip (1x) … firmware completed

Milestones
- (Dec 01) Dec 02: logic design completed … completed
- (Dec 02) Dec 03: FPGA design done … completed
- (Dec 03) Jul 04: GMT available … delay: Oct/Nov 04
- (Jun 04) Oct 04: GMT tested … delay: Nov/Dec 04
- Oct 04: GMT integration tests start … delay: Jan 05
- Jan 05: GMT integration tests completed (RPC, DT, CSC)
Proposal for Integration tests

- GMT Logic board needs GT crate
  - Due to complex custom backplane, it is not compatible with a standard VME slot
- Planning to ship a GT crate to CERN before the end of the year
  - Install in Prevessin Test Center
- Propose to do integration tests at CERN when GMT board is ready
  - starting Jan 05
GMT will use same software structure as Global Trigger

- Boards are in the same crate & use same controller

- SW that directly accesses hardware will run in XDAQ framework

GMT Online Software Concept

1) Edit and register configuration (before run)
2) Tag a configuration (e.g. RUN1567) (before run)
3) Configure with tag RUN1567 Just before starting run
4) Retrieve configuration RUN1567 & configure hardware

Online SW on PC in rack (XDAQ)
- C++ classes for Chips, Boards
- can be used standalone (testing, …)
- can be used via SOAP interface (e.g. by Run Control or by private interface)

Configuration Editor GUI
Configuration Selection GUI
Run Control

Config DB

Status
JTAG Access Library (JAL)

- Started with a sub-project: JTAG Access Library
  - Need to program flash PROMs in place (via VME)
  - Same problem in DT, GMT, GT and in other (trigger) components

- Developed a generic solution via JTAG
  - Program/configure PROMs/FPGAs
  - Do any other JTAG operation
    - SPY / local DAQ (if foreseen through JTAG)
    - Boundary Scan
  - Works with Xilinx and Altera PROMs / FPGAs
  - Uses the Hardware Access Library (HAL) to access a JTAG chain via VME
  - Works with Standard Vector Format (SVF) files
    - Xilinx and Altera flavors
JTAG Access Library (JAL)

PC running XDAQ

JTAG Controller
Device (e.g. ScanPSC100F) or firmware mapped into VME address space

JTAG Chain
Containing Altera or Xilinx Devices

JTAG Access Library as a component of the online software

XDAQ Application running on PC in Rack

Monitoring Test GUI Run Ctrl Config DB

DB Interface

Test / Local Control

Configuration

Monitoring / Spy

JAL

Hardware Access Library

DB Interface

Run Ctrl

Test GUI

Config DB
JTAG Access Library (JAL)

- C++ library to access JTAG chains in hardware
  - Supports multiple JTAG controllers on a board/crate, multiple chains
  - Multithreading support foreseen (multiple chains on one controller used concurrently)
  - ready for the XDAQ framework

- Multiple ways to access JTAG chain
  - JAL ⇒ Hardware Access Library (HAL) ⇒ PCI-VME ⇒ JTAG controller chip
  - JAL ⇒ Parallel port cable (e.g. ByteBlaster)
  - JAL ⇒ other access methods (e.g. PCI; easy to extend)

- Supports different JTAG Controllers (via VME)
  - National Semiconductor ScanPSC100
  - JTAG controller firmware (developed by J. Erö for DTTF)
JTAG Access Library (JAL)

- Classes provide easy access to the JTAG Chain
  - JTAGController (with different implementations)
    - send TMS sequence
    - scan bits through chain
  - JTAGChain
    - Scan Instruction Registers
    - Scan Data Registers
    - Change state …
  - JTAGSVFSequencer
    - Sequence a Standard Vector Format File (SVF)
    - Format supported by both Xilinx and Altera tools
    - Program/Verify PROMs

The model of the JTAG state transitions and ScanPSC100 controller are based on C code from National Semiconductor Corp. with changes by Florida CMS group
Many thanks to D. Acosta, A. Madorsky, H. Stoeck!
JTAG Access Library: Status

Tests

- Tested programming of Altera EPC-2 enhanced configuration devices
  - Via HAL / VME / ScanPSC100Controller
    - Works (slightly slower than Quartus II)
  - Via Parallel port & ByteBlaster Cable
    - Works (slightly slower than Quartus II)
  - Multiple devices programmed in parallel (time saving)
  - Tests done at UAM Madrid with DTTF tester board.
    Many thanks to J. F. Trocóniz, M. Fernandez, J. Erö, Ch. Deldicque

Plans

- Tests with Xilinx PROMs
- Support other JTAG controllers
Summary

- Firmware of all ten FPGAs completed
  - 100% agreement between firmware and ORCA (C++) simulation

- GMT Logic Board
  - Mezzanine boards have been designed and produced
  - Schematics, Layout, Routing completed
  - Currently doing final checks
  - Production this month

- Development of on-line software started
  - JTAG Access Library (JAL) now complete