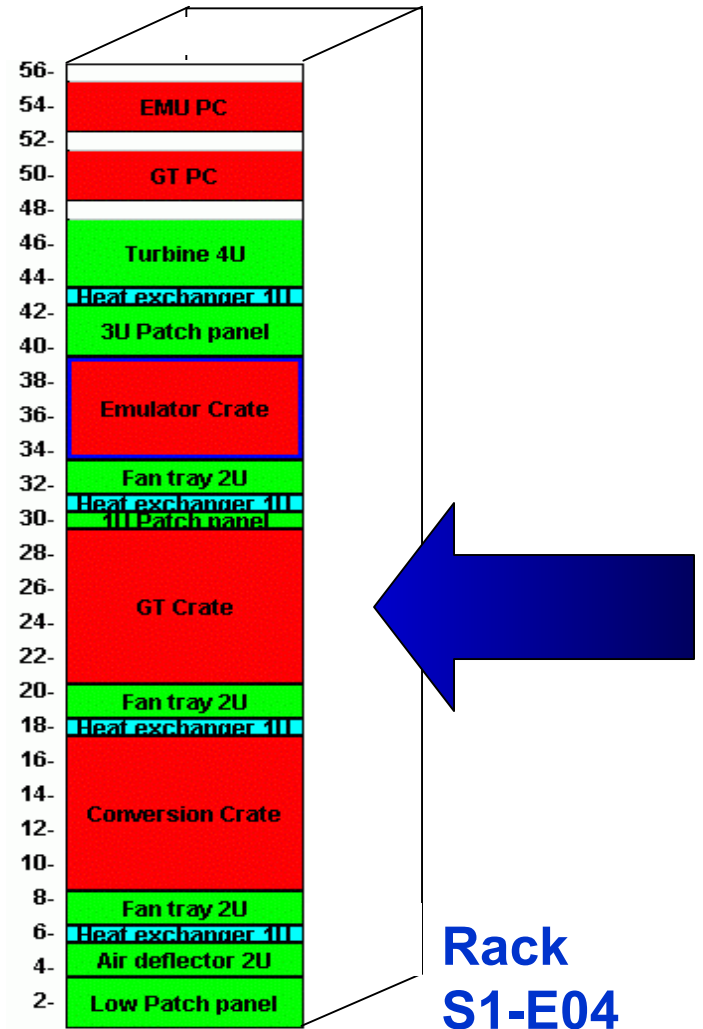
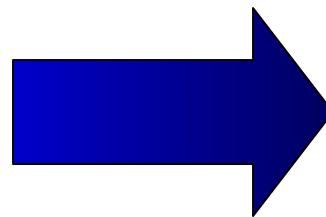
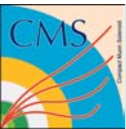


Global Muon Trigger Update

Hannes Sakulin, HEPHY Vienna

Trigger Meeting
CMS Week, CERN
9th December, 2003





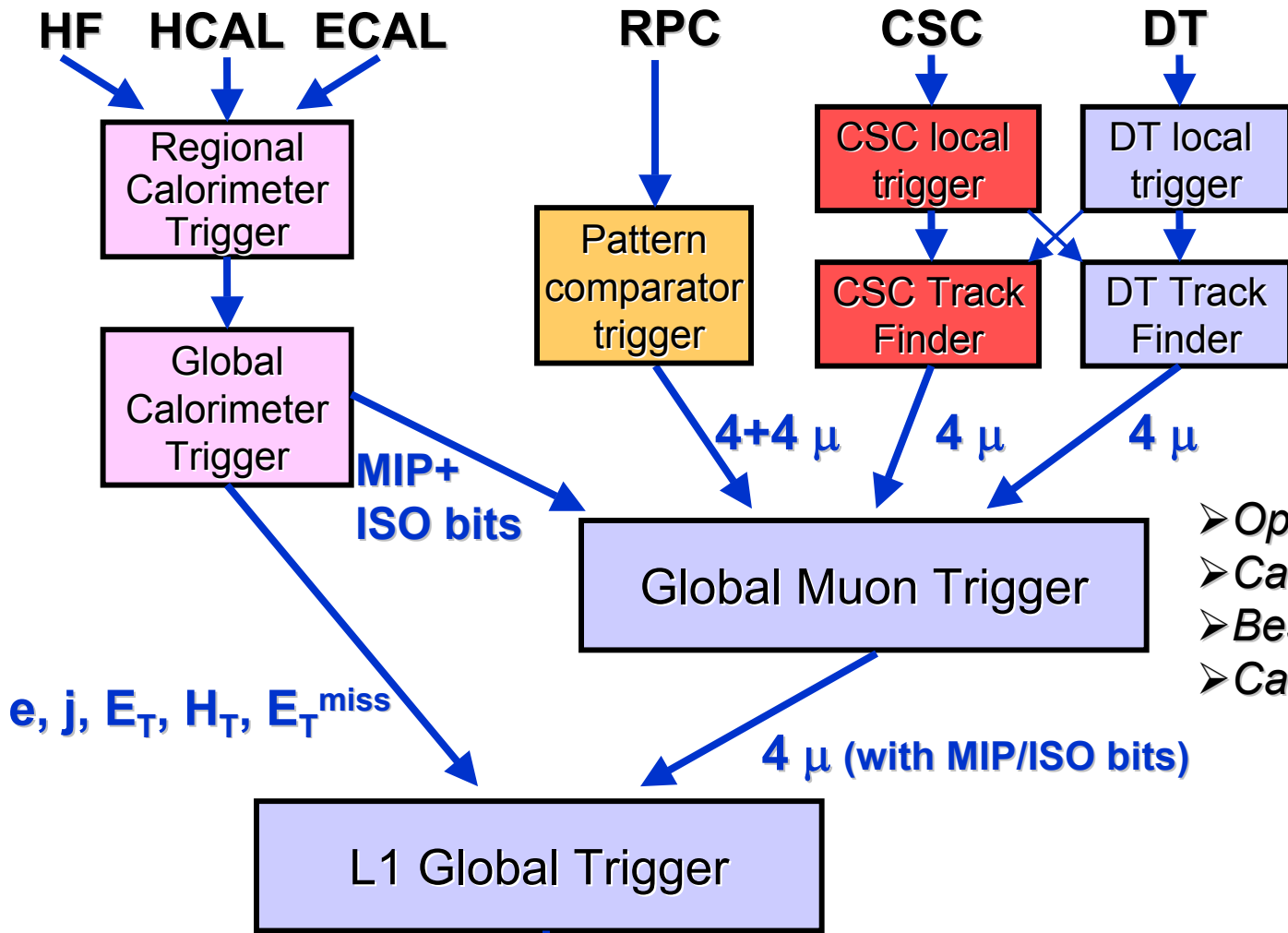
CMS Level-1 Trigger



Calorimeter Trigger

Muon Trigger

Pipelined 40 MHz, Latency < 3.2 μs

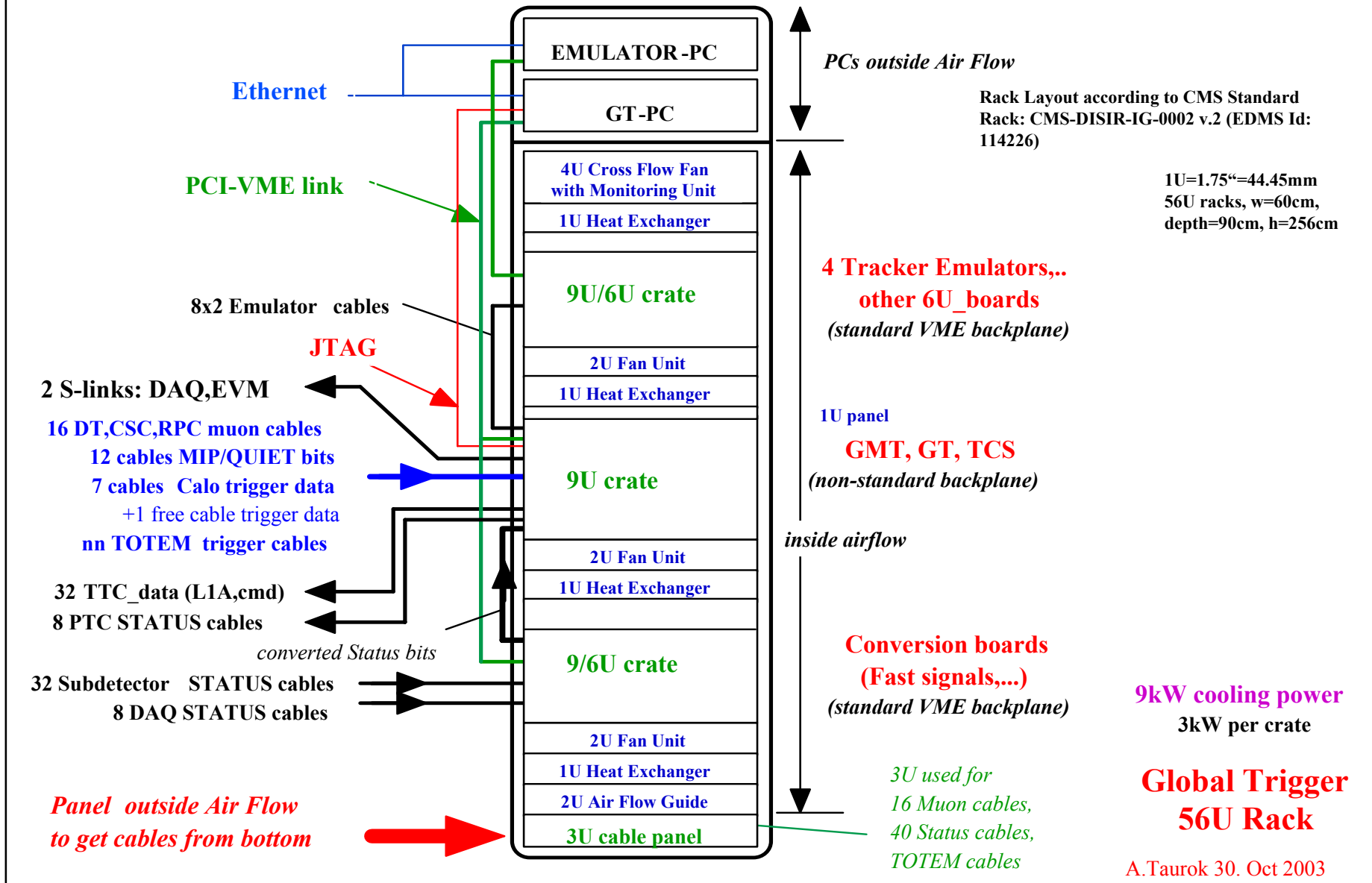


- *Optimal Combination*
- *Cancel out duplicates*
- *Best four muons*
- *Calo confirmation + isolation*

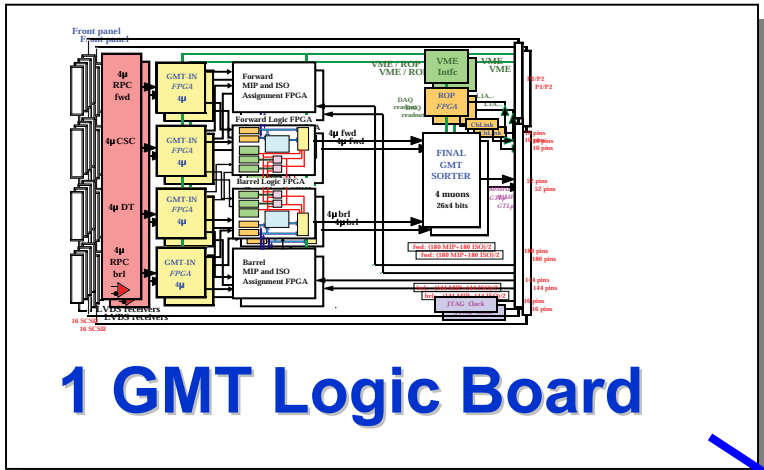
max. 100 kHz

L1 Accept

Global Trigger Rack



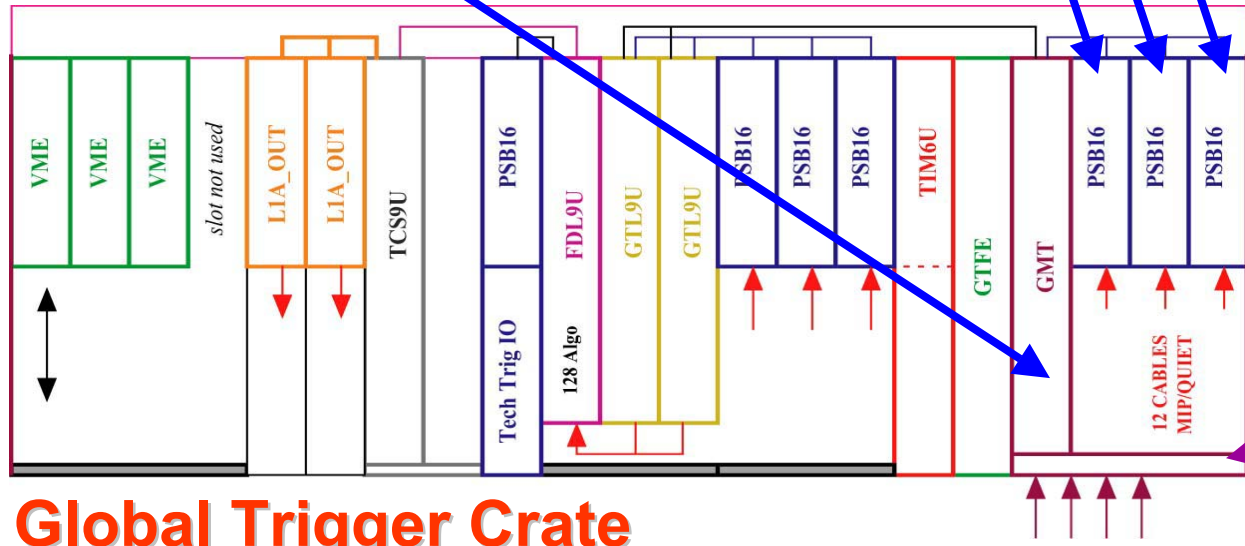
GMT in the Global Trigger Crate



Conceptual design ready
FPGAs being designed



6-channel
prototype
available

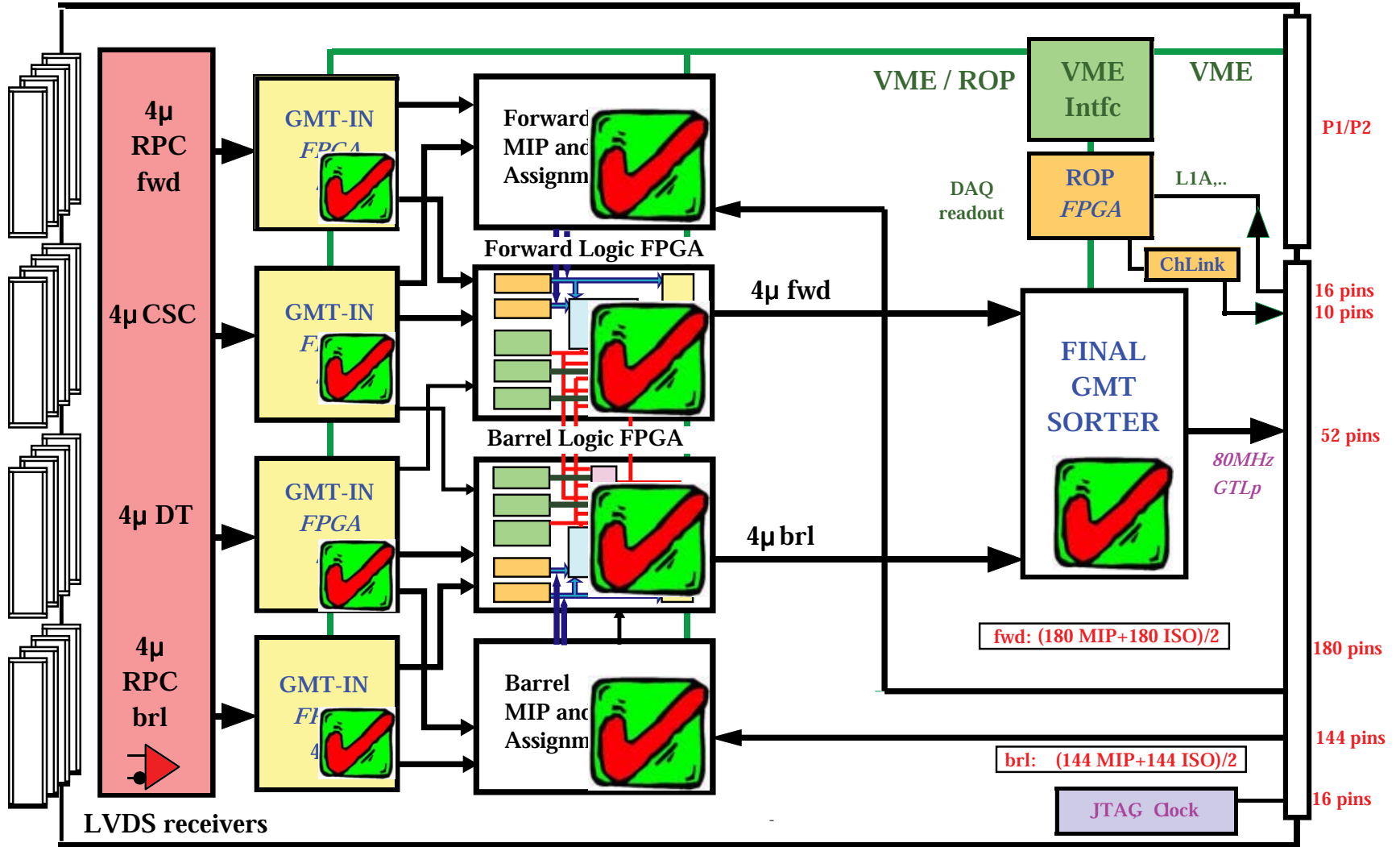


4 DT/CSC + 8 RPC muons

Special wide
input board
parallel to
front panel

Firmware done. (except readout)

Front panel



16 SCS12

➤ New: Input FPGAs

- ⇒ Over-sampling at 160 MHz
- ⇒ Programmable delay line
- ⇒ TBD: readout logic

➤ New: Sort FPGA

- ⇒ Sort logic as in Logic FPGA
- ⇒ Double data rate output 80 MHz GTL+ to GT
- ⇒ TBD: readout logic

➤ Logic FPGA

- ⇒ Added (optional) phi projection to vertex
- ⇒ Now using 96/96 RAM blocks
- ⇒ Now using 81% of slices in Virtex II 3000 (half of them as DPRAM)

➤ Build system

- ⇒ Deal with multiple target devices per chip

➤ Tried all chips for Virtex II and for Spartan 3 series

Chip	Virtex II 2000	Virtex II 3000		Spartan 3 2000	Spartan 3 4000
Input (4x)					
MIP/ISO Assignment (2x)			Our choice		
Logic FPGA (2x)					
Sort FPGA (1x)					



Works at 40 MHz

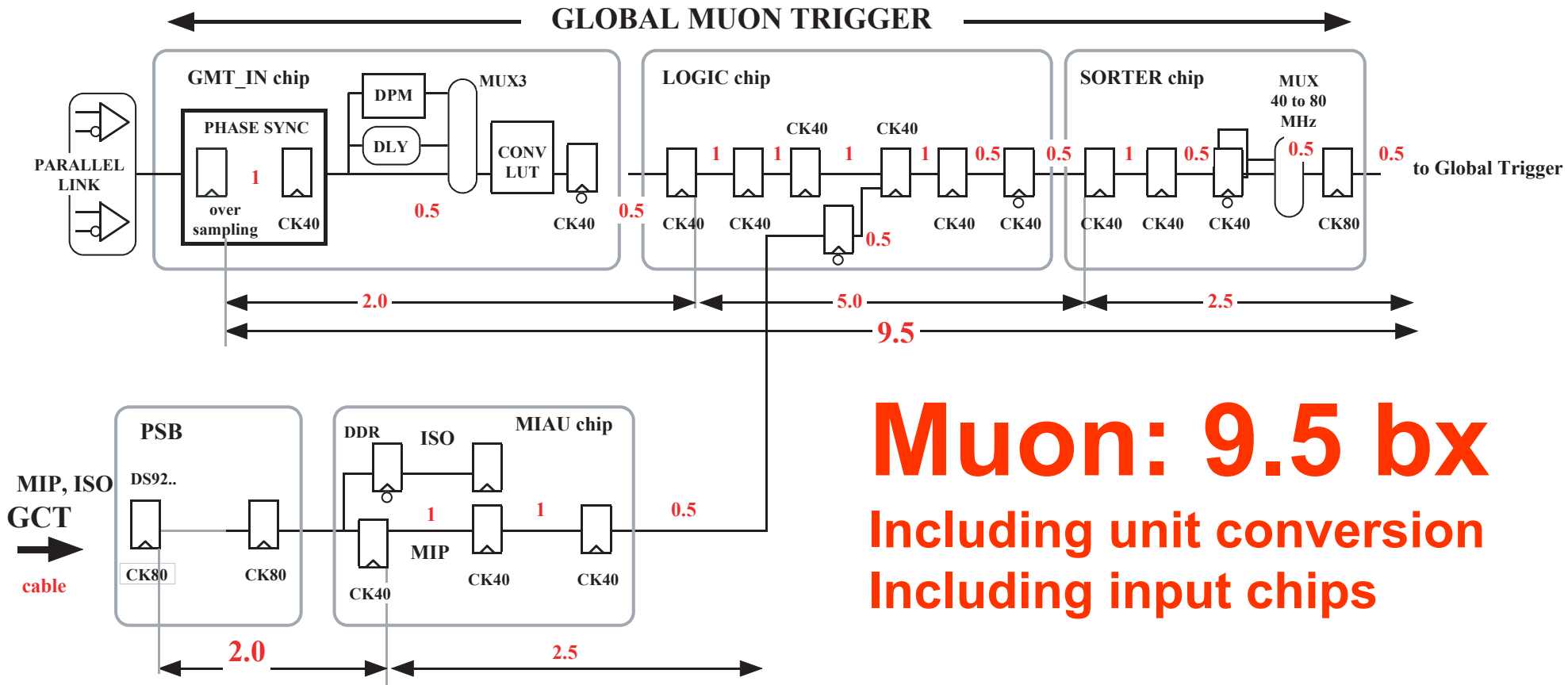


Does not fit



Too slow

- Based on timing analysis by Xilinx tools (for muons)



Muon: 9.5 bx
 Including unit conversion
 Including input chips

- L1 TriggerTDR: Muon latency ≥ 10 bx without unit conversion and without Input chips

➤ GMT consists of

- ⇒ 3 pipeline synchronizing boards ... **prototype available**
- ⇒ 1 GMT logic board ... **logic design completed**

➤ FPGA design for GMT logic board in progress

- ⇒ Input FPGA (4x) ... **firmware completed** (except readout logic)
- ⇒ MIP and ISO assignment unit (2x) ... **firmware completed (brl+fwd)**
- ⇒ GMT logic FPGA (2x) ... **firmware complete (brl+fwd)**
- ⇒ Sorter FPGA (1x) ... **firmware completed** (except readout logic)

➤ Milestones (unchanged since Apr 2002)

- ⇒ (Dec 01) **Dec 02**: logic design completed ... **completed**
- ⇒ (Dec 02) **Dec 03**: FPGA design done ... **progress as planned**
- ⇒ (Dec 03) **Jun 04**: GMT available ... **progress as planned**
- ⇒ (Jun 04) **Oct 04**: GMT tested ... **progress as planned**
- ⇒ **Oct 04**: GMT integration tests start
- ⇒ **Jan 05**: GMT integration tests completed (RPC, DT, CSC)

- Updated version of ORCA to be released soon

- Internal changes
 - ⇒ All algorithms work bitwise compatible to hardware
 - ⇒ All floating point calculations are encapsulated in LUTs
 - Input and output coded as in hardware
 - ⇒ GMT candidates are stored in hardware format (26 bits)
 - ⇒ Contains Muon Merger as in hardware

- New classes in interface
 - ⇒ **L1MuGMTReadoutBuffer**
 - ⇒ **L1MuGMTReadoutDataRecord**
 - ⇒ **L1MuGMTextendedCand**

- **L1MuGMTCand** contains only information that is sent from GMT to GT in hardware
 - ⇒ Data word bit coding now reflects hardware coding
 - ⇒ Quality definitions changed (again)
 - ⇒ Provide methods to interpret quality code
 - `useInSingleMuonTrigger()`
 - `isMatchedCand()`
 - ...
- Extended muon candidate information provided via **L1ROU** as **L1MuGMTExtendedCand**
 - ⇒ `L1ROU` ⇒ `L1MuGMTReadoutBuffer` ⇒ `L1MuGMTReadoutDataRecord` ⇒ `L1MuGMTExtendedCand`
- More configuration options in `.orcarc`
 - ⇒ E.g.: `L1GlobalMuonTrigger:MergeMethodEta = takeDT, takeRPC, byRank, byMinPt, byCombi, Special`

- **Firmware development is close to completion**
 - ⇒ **Board level VHDL simulated and cross-checked with ORCA**
 - ⇒ **Only readout-logic to be completed**

- **Choice of FPGAs**
 - ⇒ **Input FPGAs: move to new Xilinx Spartan 3 series**
 - ⇒ **Other FPGAs: stay with Xilinx Virtex II series**

- **ORCA: new release close to completion**
 - ⇒ **Bit-wise compatible to hardware**
 - ⇒ **Implements Readout Unit**
 - ⇒ **Some changes for the user of L1 Trigger Code**
 - ⇒ **to be released soon**