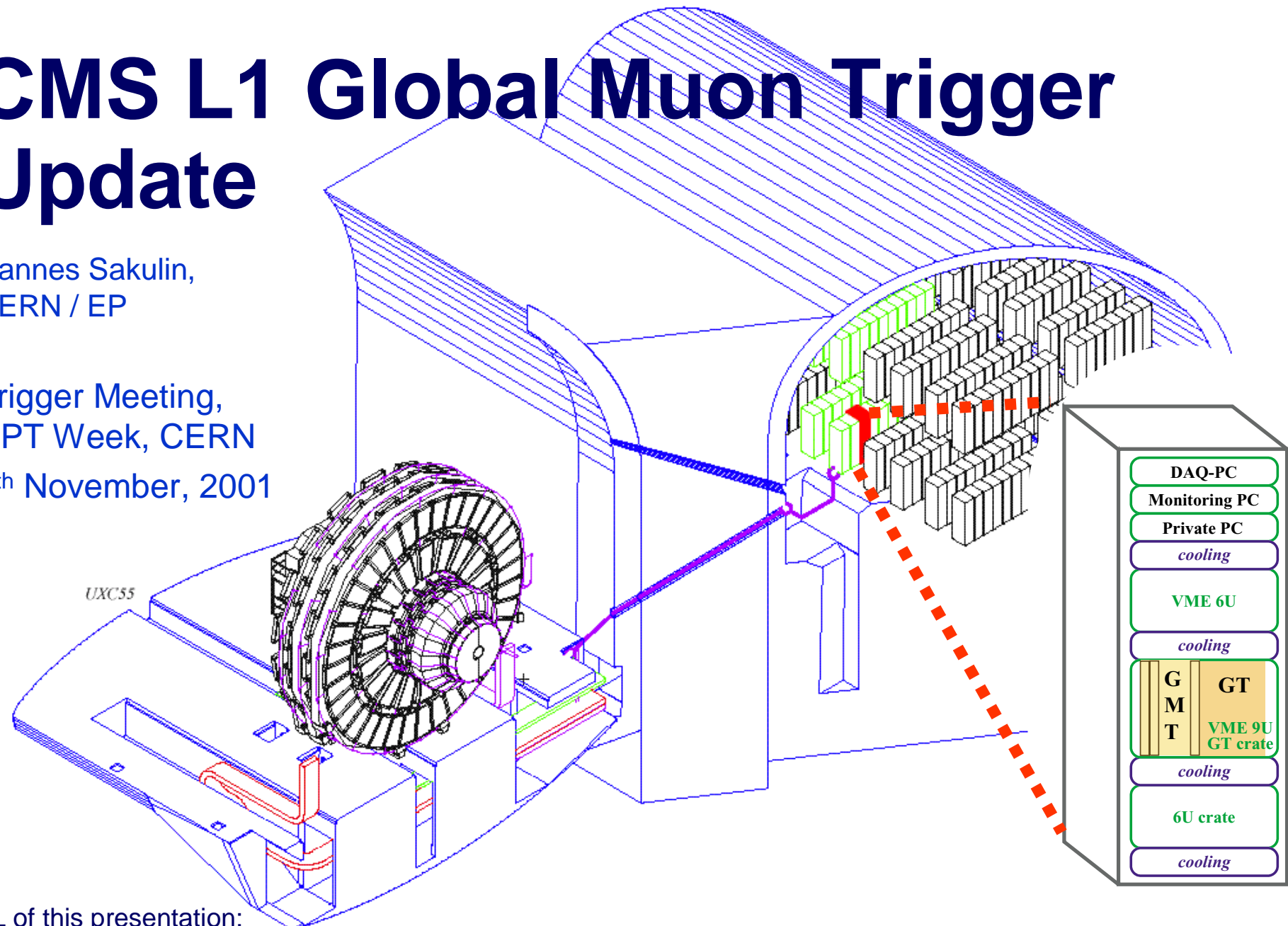


CMS L1 Global Muon Trigger Update

Hannes Sakulin,
CERN / EP

Trigger Meeting,
CPT Week, CERN
6th November, 2001

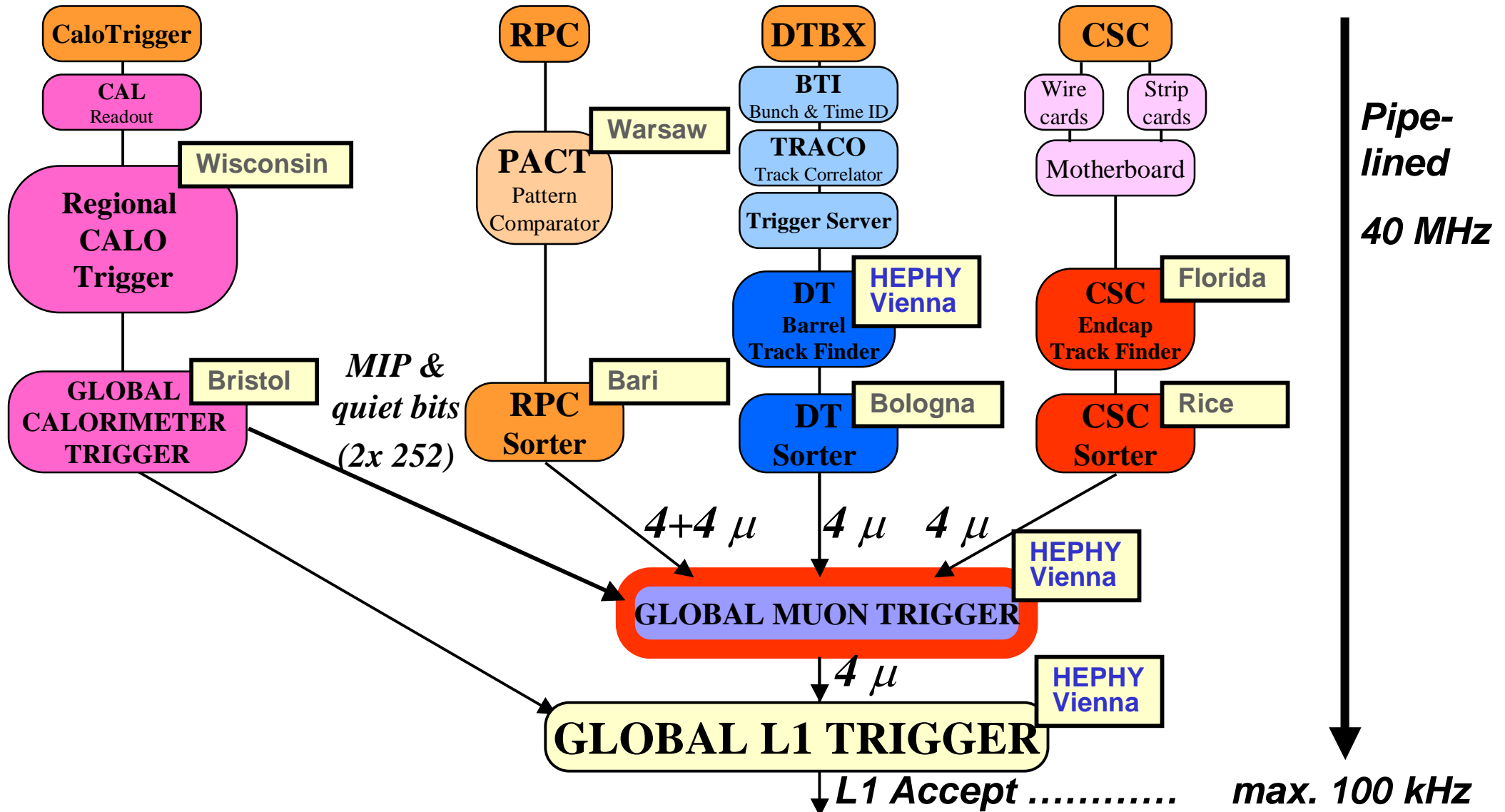


URL of this presentation:

<http://wwwhephy.oeaw.ac.at/p3w/cms/trigger/globalMuonTrigger/trans/GMT-CPTWeek06Nov2001.pdf>



CMS Level-1 Trigger

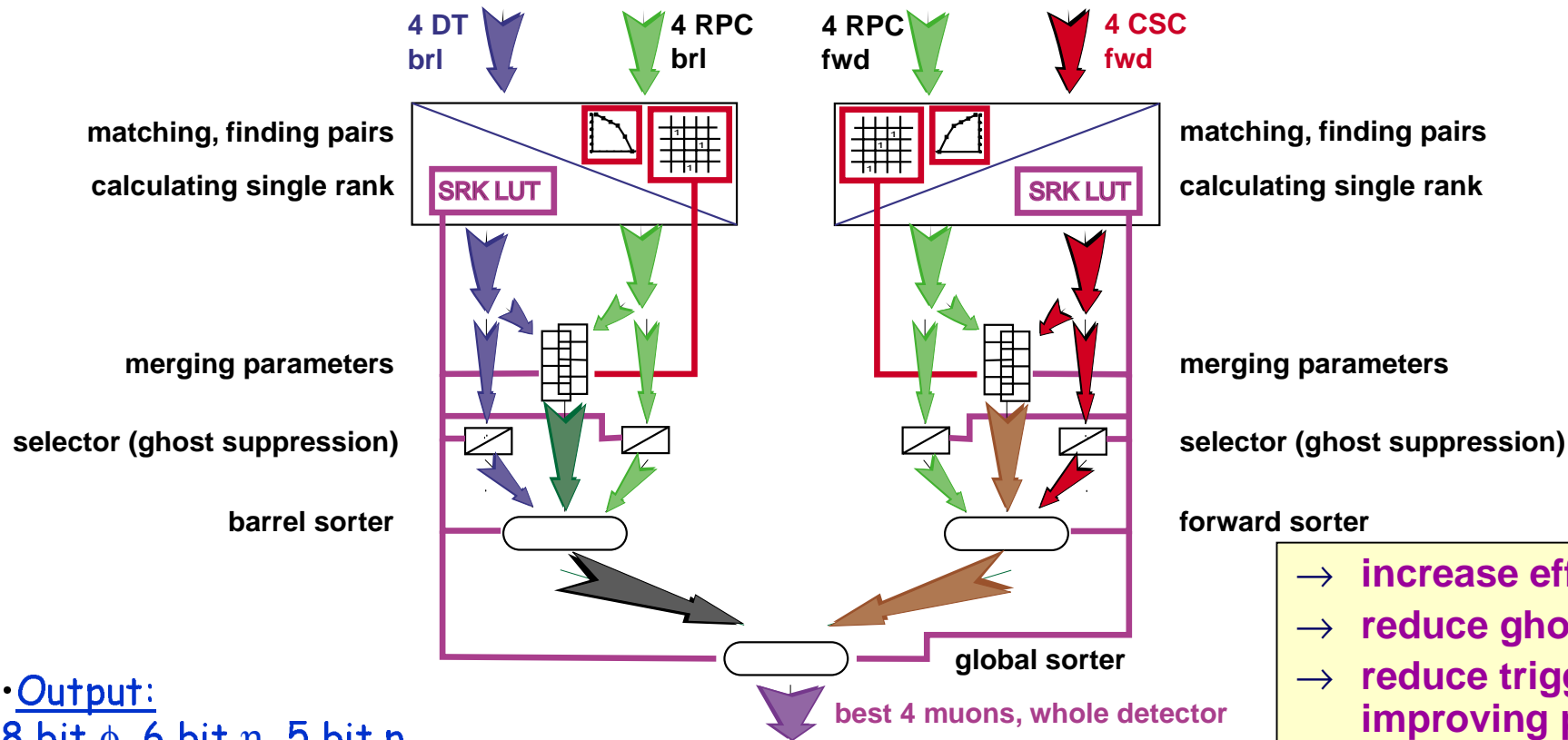


• Inputs:

8 bit ϕ , 6 bit η , 5 bit p_T ,
1 bit charge, 3 bit quality

• Further Inputs:

MIP and Quiet Bits of
252 calorimeter regions



• Output:

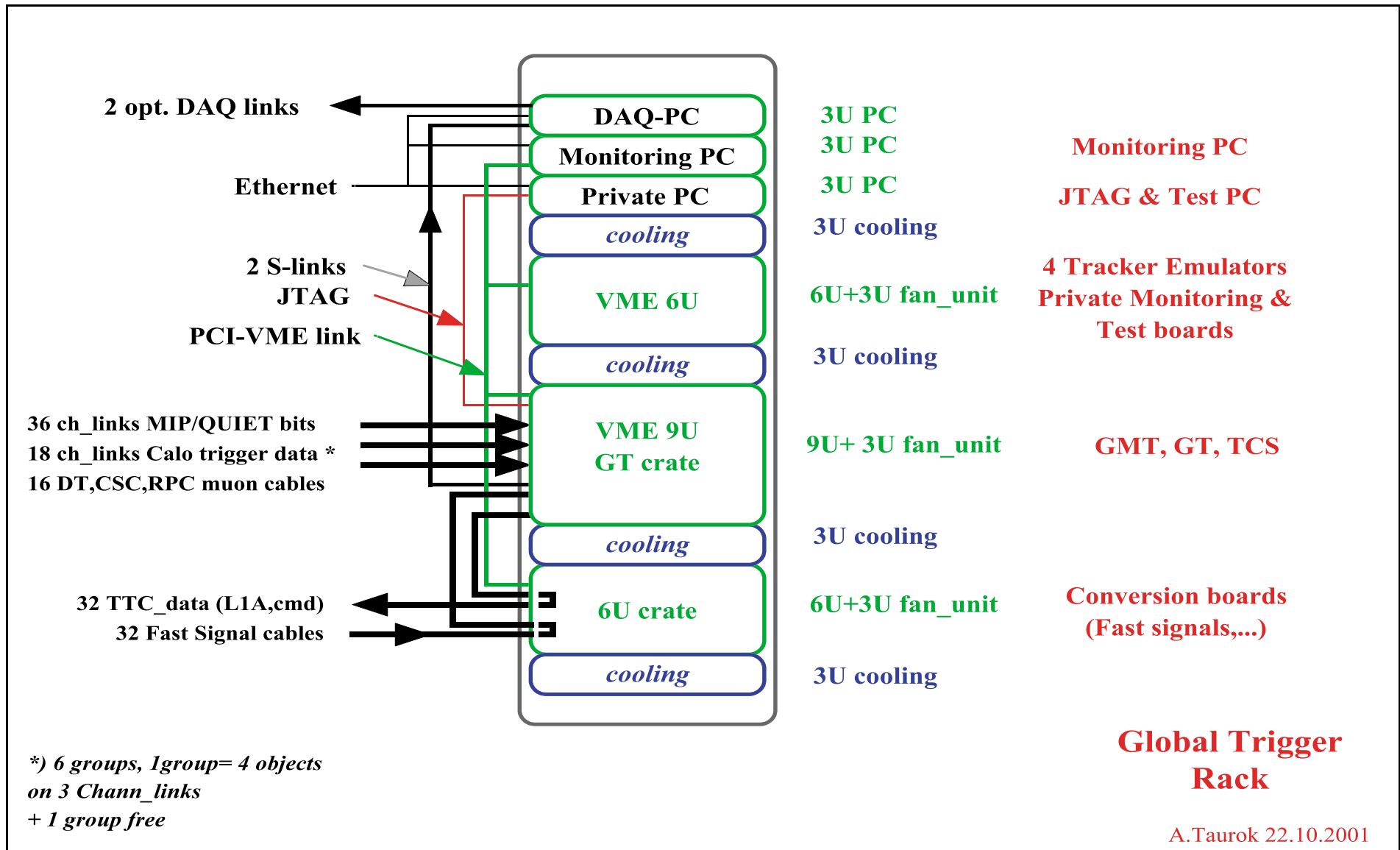
8 bit ϕ , 6 bit η , 5 bit p_T ,
1 bit charge, 3 bit quality,
1 bit MIP, 1 bit Isolation

Best 4 μ

- increase efficiency
- reduce ghosts
- reduce trigger rate by improving p_T assignment
- add MIP & ISO bits from calorimeter



The Global Trigger Rack

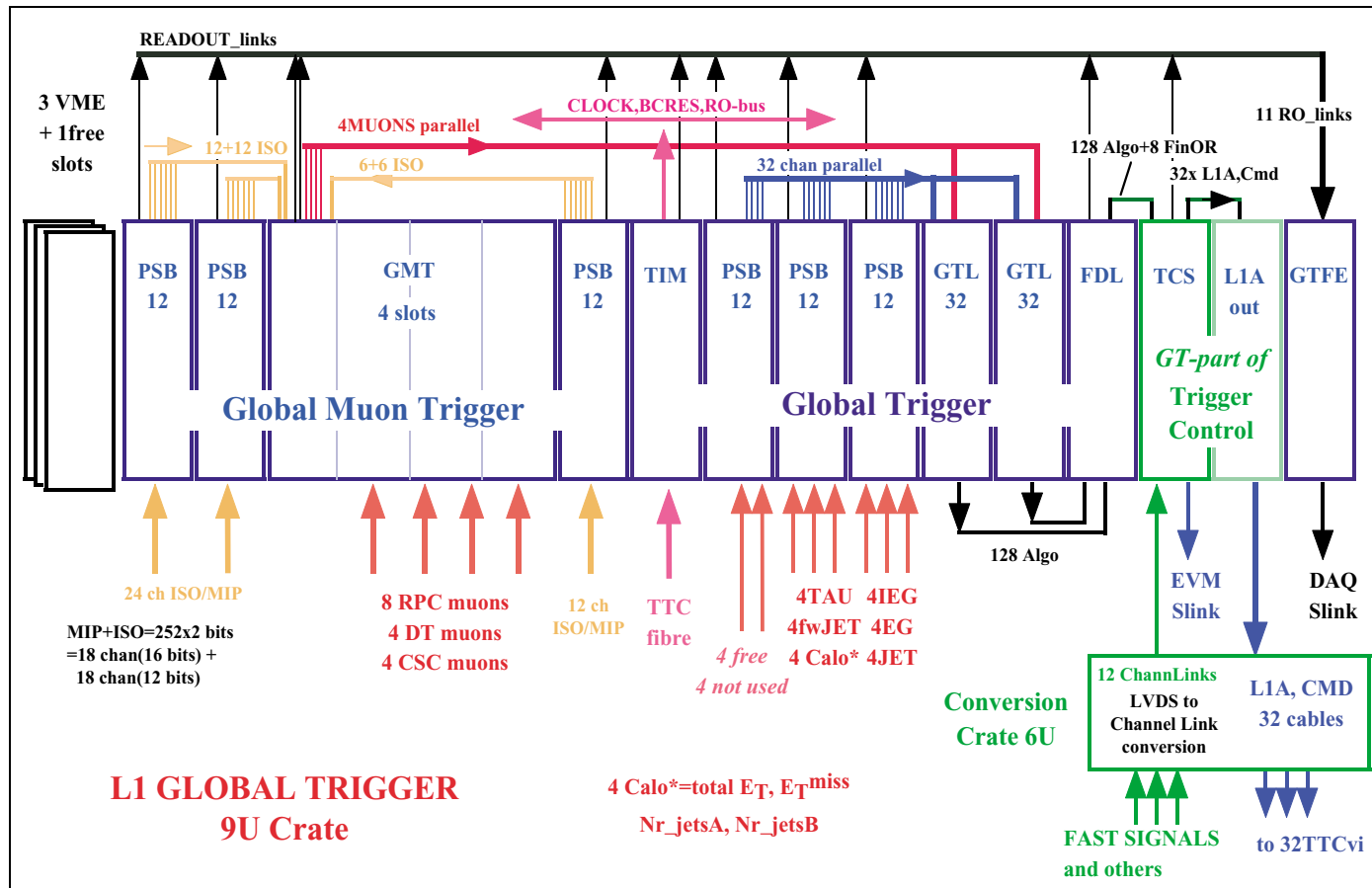




GMT in the Global Trigger Crate

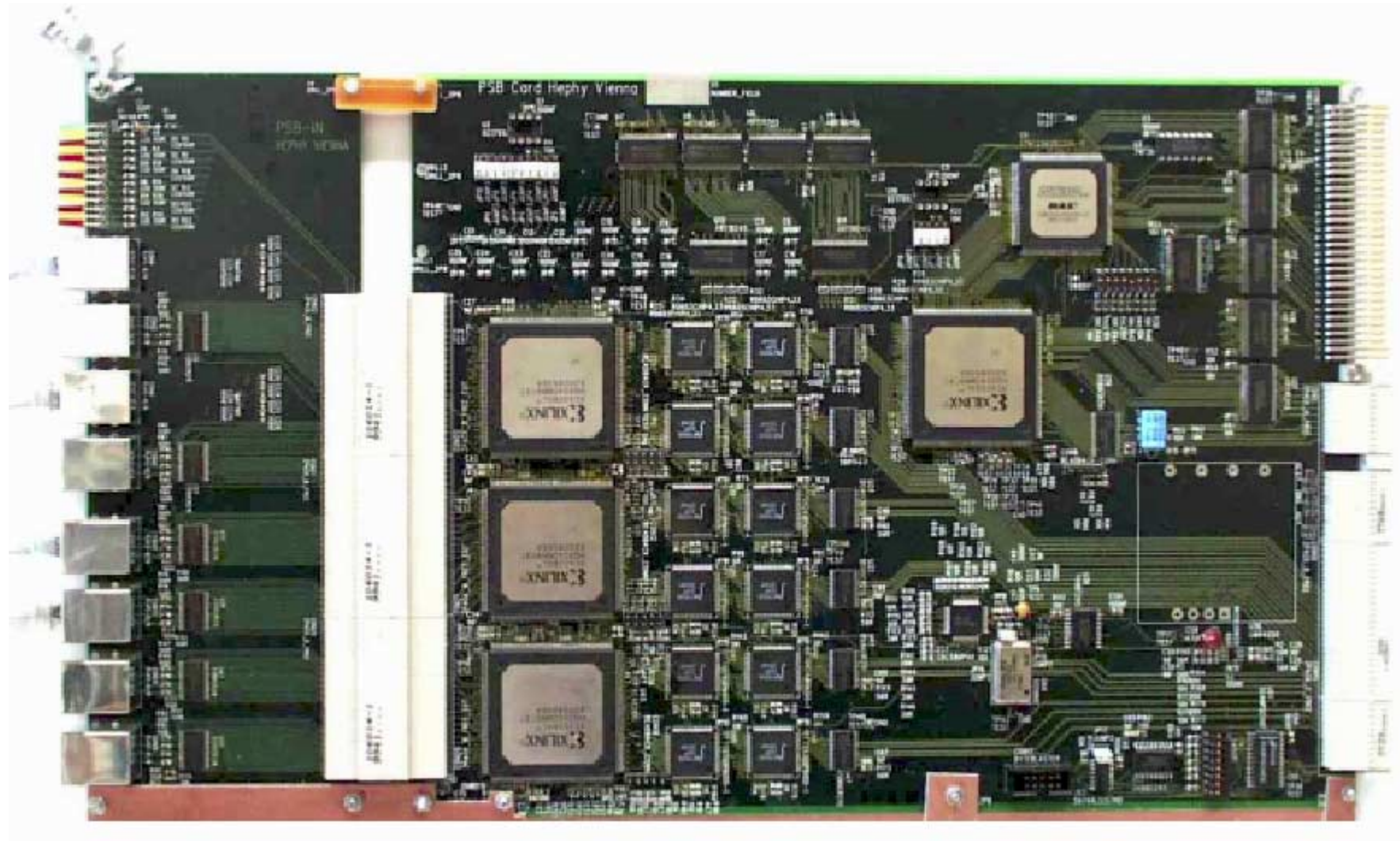


- ⇒ 1 GMT Logic Board (front panel 4 slots wide)
- ⇒ 3 PSB boards to receive calorimeter information



Sept 01

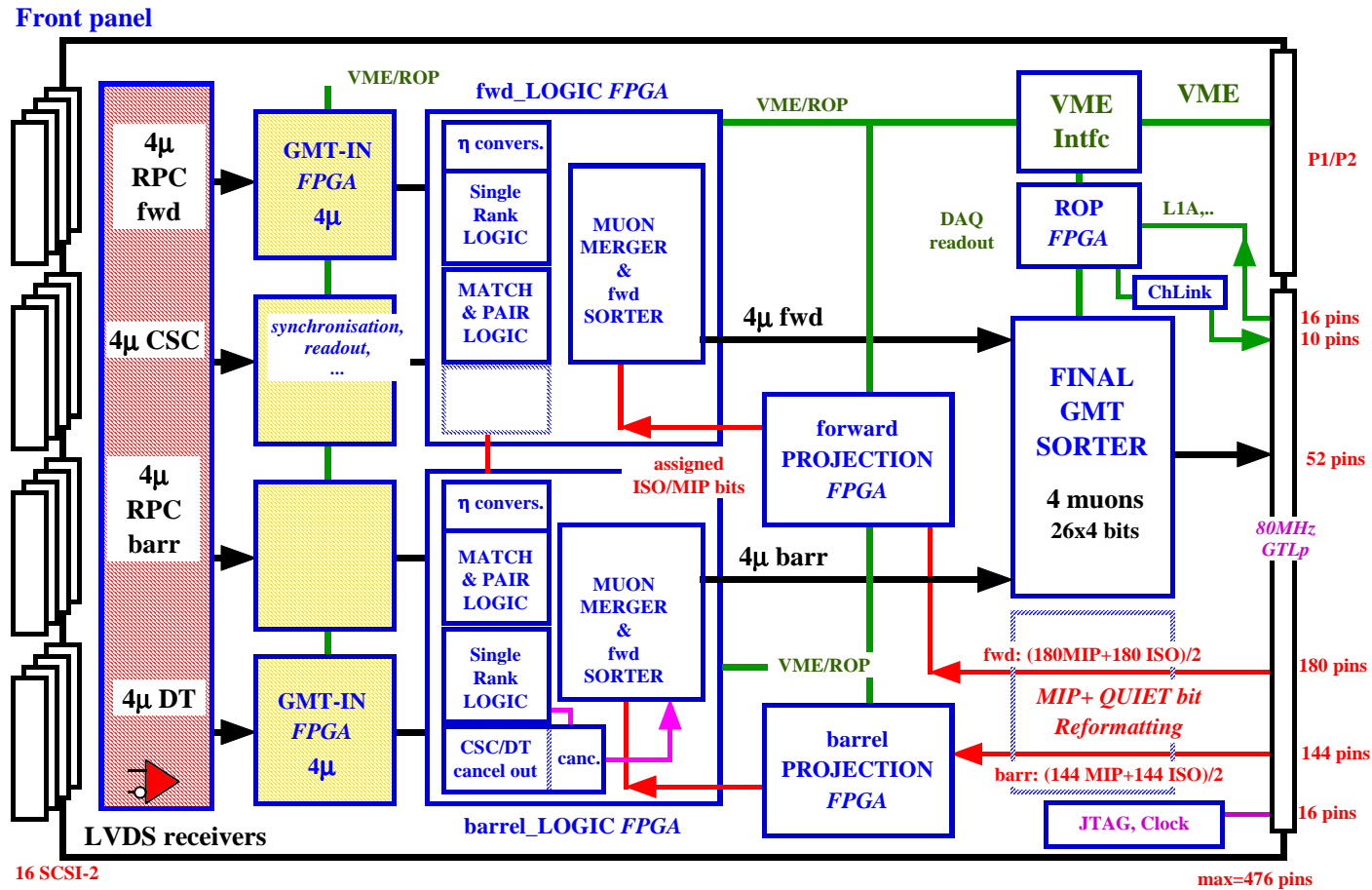
PSB 6 channel prototype



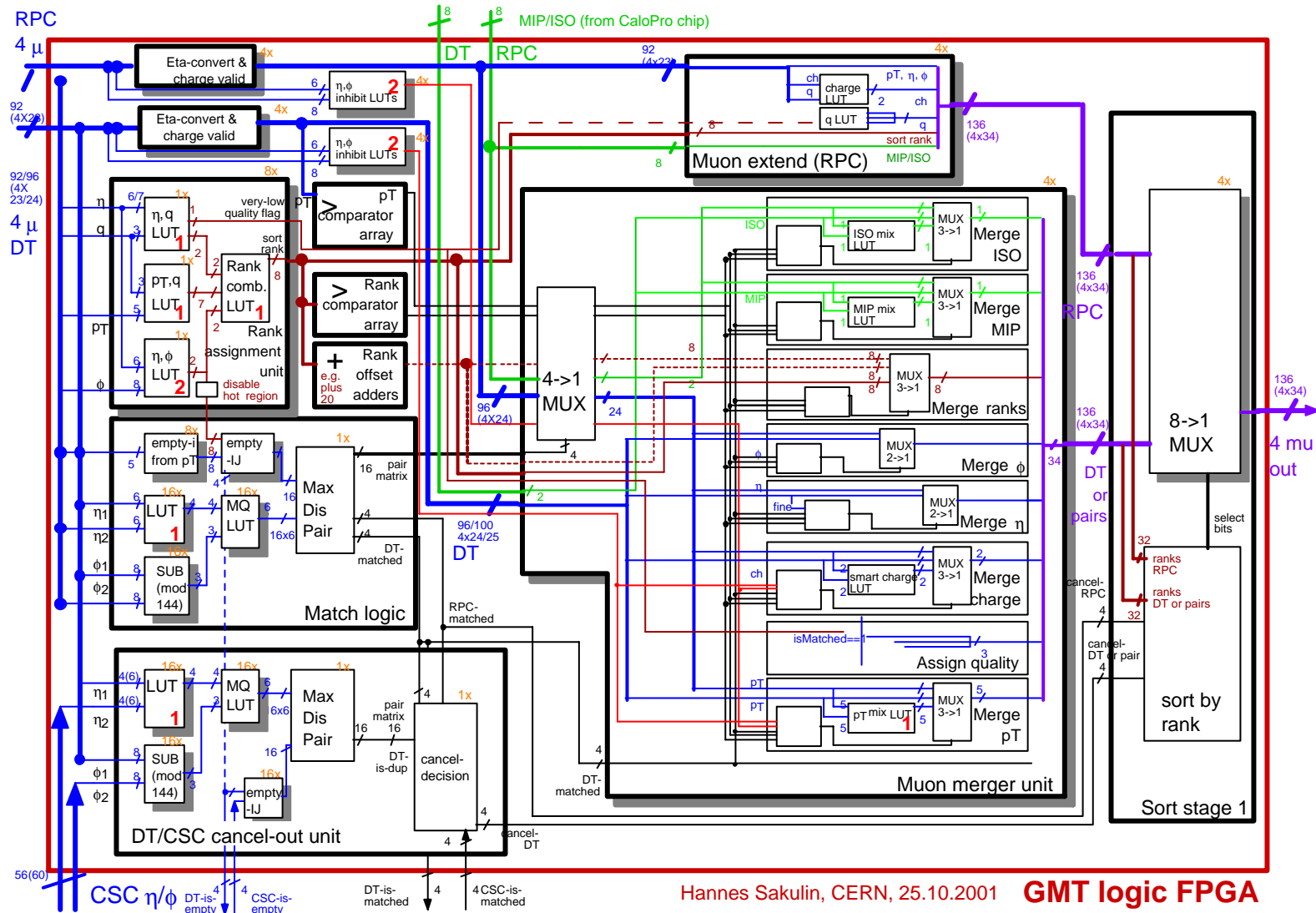
Prototype available

Latency: 14 bx

Single board Global Muon Trigger



Logic design close to completion



Hannes Sakulin, CERN, 25.10.2001 **GMT logic FPGA**

Logic design close to completion



Beam Halo Muon Trigger



- GMT input
 - ⇒ CSC halo muon candidates flagged by a halo-bit (halo muons are not seen by RPC)
- GMT operation & output to Global Trigger
 - ⇒ give high priority (rank) to halo muons
 - ⇒ assign special quality code
- Global Trigger runs algorithms to trigger calibration events
 - ⇒ **type 1**: trigger on halo muon in one endcap
 - ⇒ **type 2**: trigger on halo muon found in both endcaps
 - topological condition: match ϕ and possibly $|\eta|$ or radius
 - open question of timing
 - ⇒ trigger only on **type 2** halo muons to reduce the rate if necessary
- Beam Halo trigger is possible during normal physics data taking (from point of view of GMT)



GMT Hardware schedule



ID	Task Name	98	1999		2000		2001		2002		2003		2004		2005	
			H1	H2	H1	H2	H1	H2	H1	H2	H1	H2	H1	H2	H1	H2
1	GMT Conceptual Design				[Red bar]											
2	GMT simulation, logic design				[Red bar]											
3	GMT FPGA design						[Red bar]									
4	GMT production								[Red bar]							
5	GMT available															
6	Finish delivery															◆ 25/2
7	Online Software											[Pink bar]				
8	Finish commissioning															◆ 1/7

➤ Milestones / Plans:

- ⇒ 2001 Logic design, ORCA + VHDL Simulation
- **Dec 2001** Logic design finished
- ⇒ 2002 VHDL Simulation, Design of FPGA chips
- **Dec 2002** FPGA design finished
- ⇒ 2003 Production of VME 9U Boards
- ⇒ 2004/05 Integration tests, production of spare boards



Progress in 2001 & Plans for 2002



➤ Progress in 2001:

- ✓ Logic design close to completion
 - Chip Models selected (mostly Virtex II), Interconnections defined
 - Design compacted (external RAMs moved into big FPGAs)
 - Detailed GMT design document
 - ✓ Improvement of functionality
 - DT/CSC cancel-out unit (improved performance in barrel/endcap overlap region)
 - ✓ in parallel:
 - ORCA Simulation extended and improved
 - Continuous studies to optimize GMT design parameters and performance
- ⇒ VHDL behavioral level simulation has started

➤ Plans for 2002:

- ⇒ continue VHDL simulation of FPGA chips
- ⇒ VHDL simulation of GMT board
- ⇒ Synthesis / design of FPGAs
- ⇒ in parallel further studies with ORCA

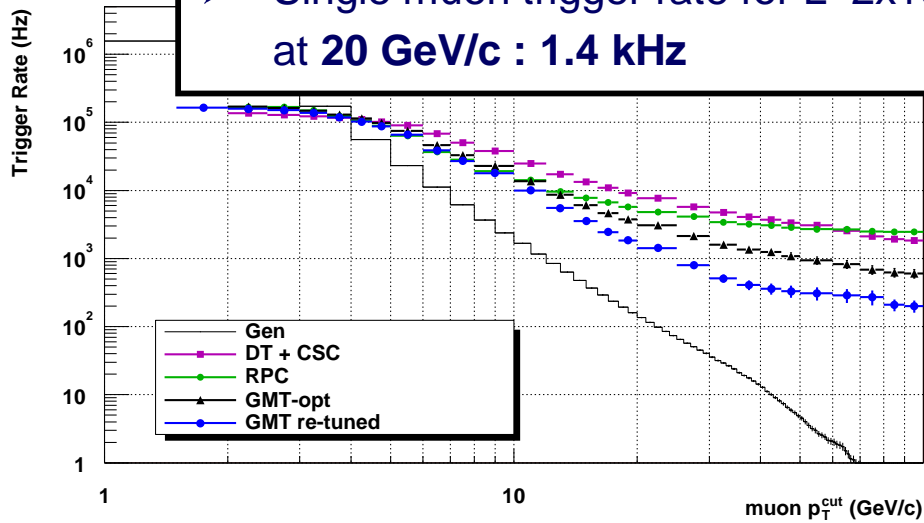


Simulation results

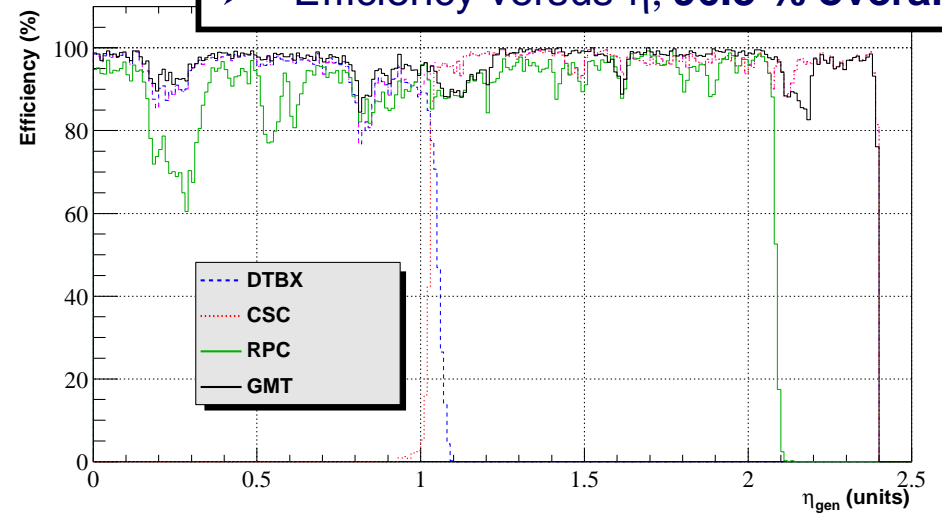
muon 2001 production, ORCA 5.1.2



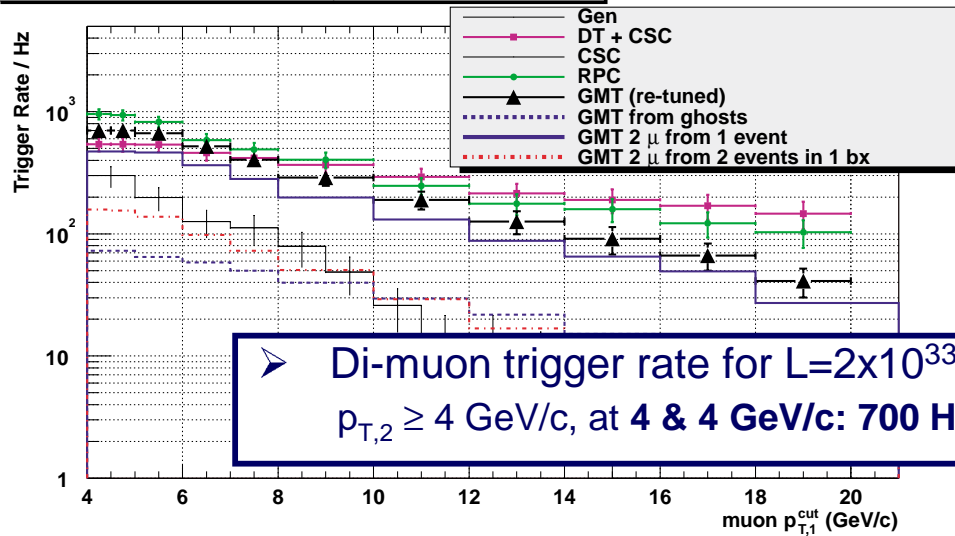
➤ Single muon trigger rate for $L=2 \times 10^{33}$ at 20 GeV/c : 1.4 kHz



➤ Efficiency versus η , 96.3 % overall

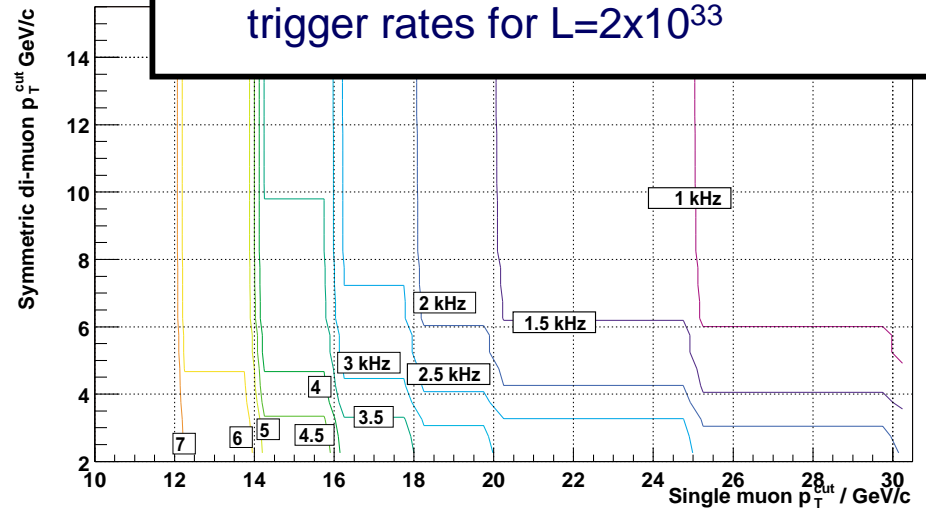


Di-muon Rates - $p_{T,2} \geq 4$ GeV/c



➤ Di-muon trigger rate for $L=2 \times 10^{33}$ $p_{T,2} \geq 4$ GeV/c, at 4 & 4 GeV/c: 700 Hz

➤ Single muon / di-muon combined trigger rates for $L=2 \times 10^{33}$





Conclusion



- Progress in hardware design as planned
 - ⇒ logic design almost completed
 - FPGAs selected
 - design compacted & improved
 - ⇒ new solution with 1 logic board
 - ⇒ trigger on halo muons is possible during normal physics running (from GMT point of view)
- Planned R&D in 2002
 - ⇒ VHDL simulation of FPGAs and board
 - ⇒ design of FPGAs
- Simulation results with 2001 muon production
 - ⇒ p_T -cut was lower than in last year's production
 - ⇒ improved CSC trigger & GMT can cope with higher background rate
 - ⇒ updated results with higher statistics expected by the end of the year