

Global Muon Trigger status & plans

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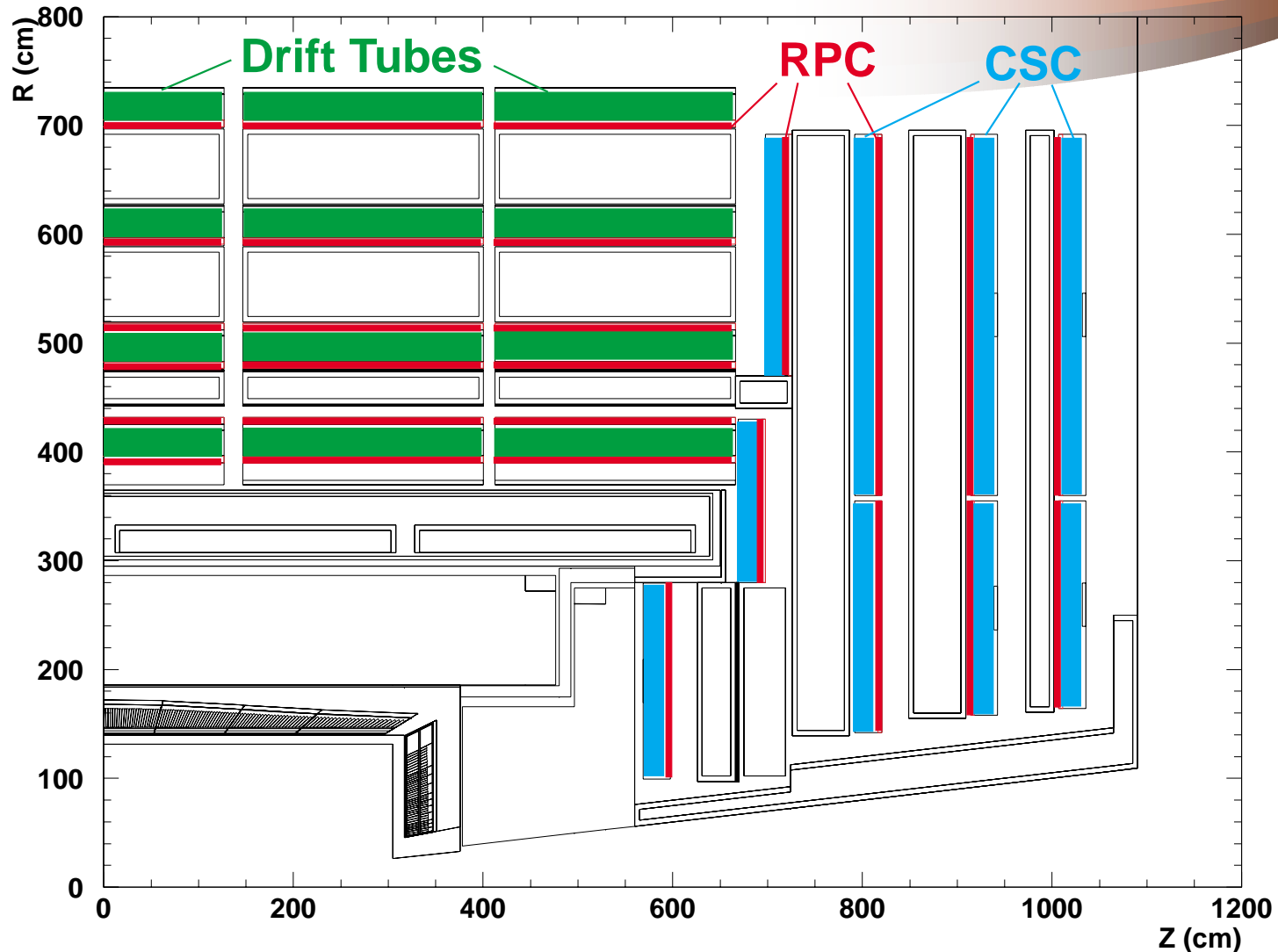
Global Muon Trigger - Overview



- Introduction
- Hardware
 - progress in logic design
 - design simplified
- Simulation
 - ORCA 4.5.0, CMS 121
 - Updates to software

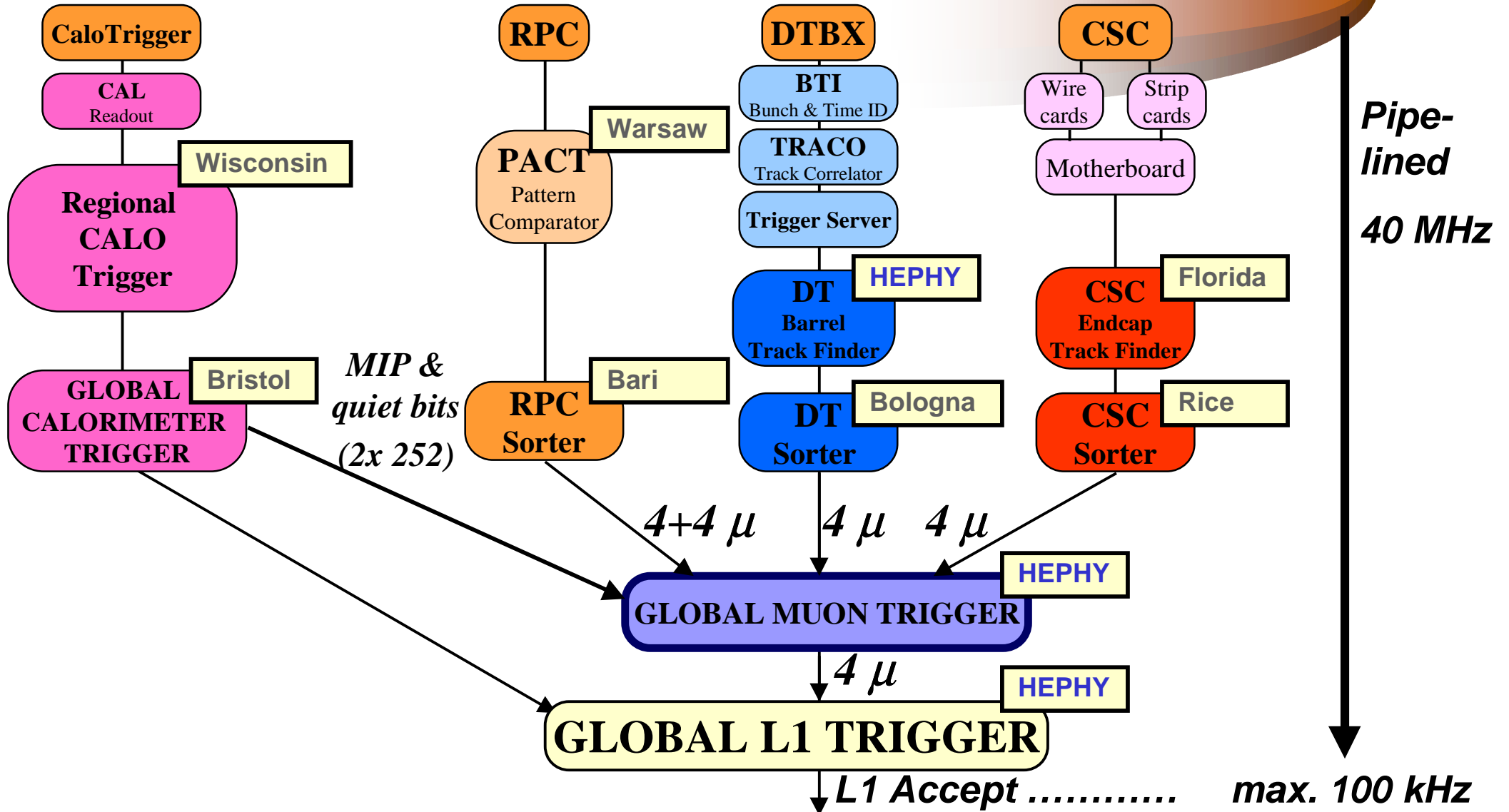


CMS Muon System





CMS Level-1 Trigger





Tasks of the GMT



- Find the best 4 muons in the detector
- Make use of the complementarity of the muon triggers (DT/RPC barrel, CSC/RPC endcap)
 - increase efficiency
 - reduce ghosts
 - reduce trigger rate by improving p_T assignment
- Add MIP and Quiet bits from the calorimeter trigger



Principle of the GMT



Inputs:

8 bit ϕ , 6 bit η , 5 bit p_T ,
1 bit charge, 3 bit quality

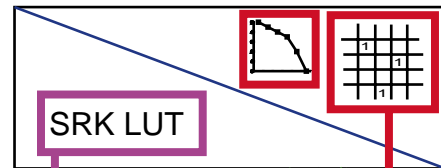
4 DT brl 4 RPC brl

4 RPC fwd 4 CSC fwd

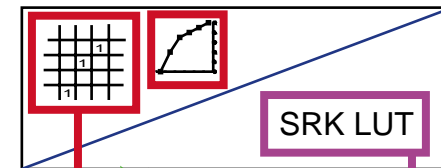
Further Inputs:

MIP and Quiet Bits of
252 calorimeter regions

matching, finding pairs
calculating single rank



matching, finding pairs
calculating single rank



merging parameters

merging parameters

selector (ghost suppression)

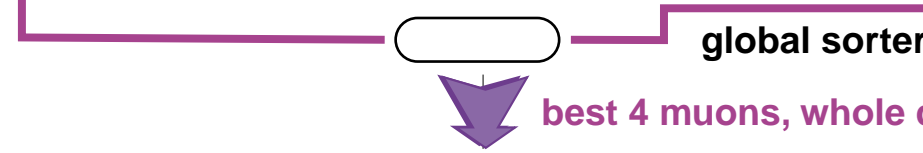
selector (ghost suppression)

barrel sorter

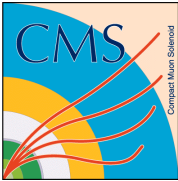
forward sorter

Output:

8 bit ϕ , 6 bit η , 5 bit p_T ,
1 bit charge, 3 bit quality,
1 bit MIP, 1 bit Isolation



best 4 muons, whole detector



GMT Hardware status



ID	Task Name	98	1999		2000		2001		2002		2003		2004		2005	
		H2	H1	H2	H1	H2	H1	H2	H1	H2	H1	H2	H1	H2	H1	H2
1	GMT Conceptual Design				[Bar]											
2	GMT simulation, logic design						[Bar]									
3	GMT FPGA design								[Bar]							
4	GMT production										[Bar]					
5	GMT available															
6	Finish delivery															◆ 25/2
7	Online Software												[Bar]			
8	Finish commissioning															◆ 1/7

↑
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- Conceptual Design has been presented (Nov 2000)
- Currently in the phase of detailed logic design
 - lots of progress: Chip Models determined, interconnects defined, ...
- Plans:
 - 2001 Logic design, ORCA + VHDL Simulation, finalize Interface Documents (drafts available!)
 - 2002 Design of FPGA Chips
 - 2003 Production of VME 9U Boards
 - 2004/05 Integration tests, production of spare boards

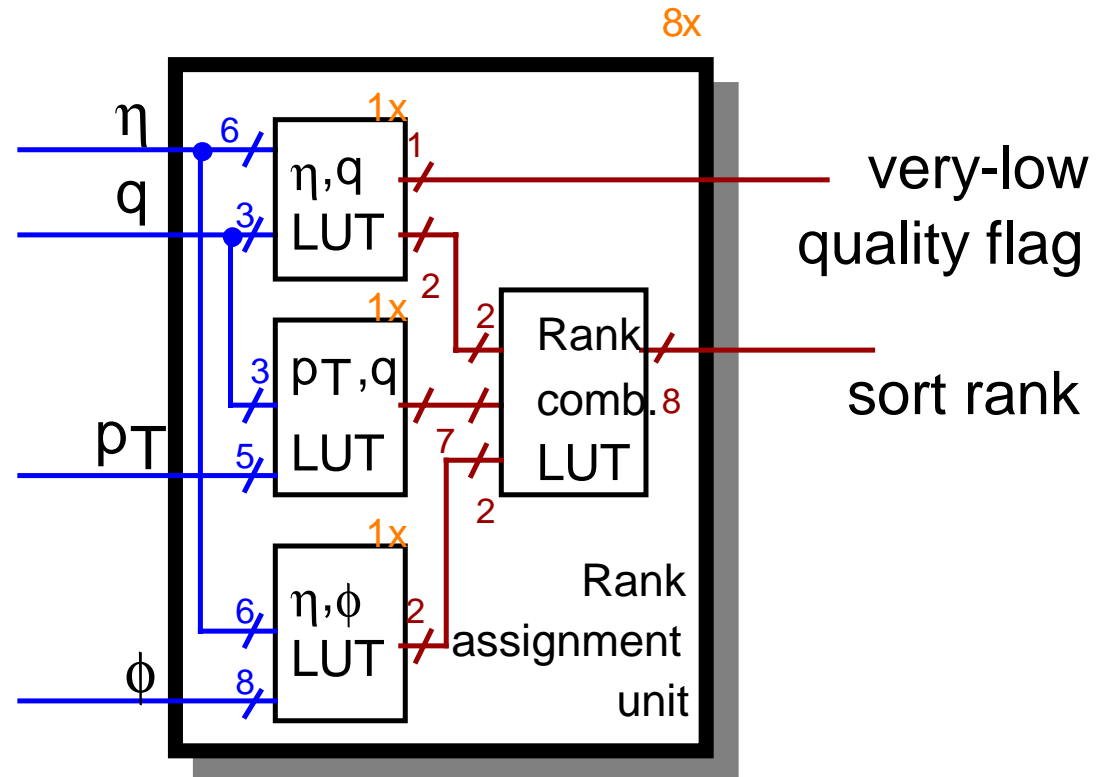
Rank assignment unit

- Now included in **GMT Logic FPGA** (Virtex XC2V3000)
 - 5 VirtexII SelectRAM blocks / muon

...modified by η , quality

Main contribution from p_T , quality

...modified by η , ϕ





Rank assignment



- ⇒ **Main rank** increases with p_T and **quality** and if matched
- ⇒ **η - ϕ modifier** to decrease rank for noisy channels or even switch them off:

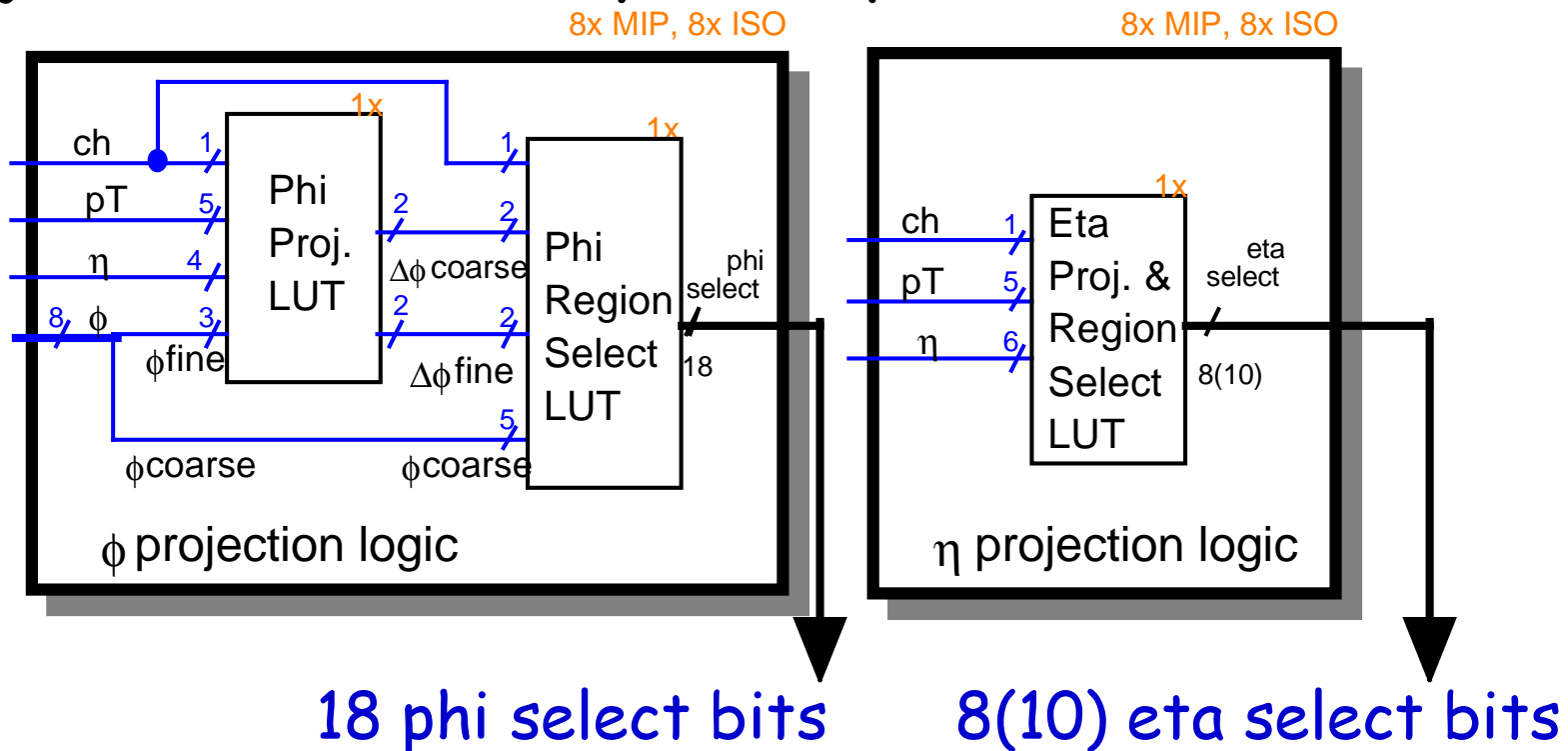
Programmable
Rank for
very low
quality

RANK	eta - phi modifier 10	eta - phi modifier 01	eta - phi modifier 01	eta - phi modifier 11
192..255	Normal from ϕ, p_T			
128..191		reduced by half scale		
64..127			reduced below all other	
0..63				
0 ... empty				switched off

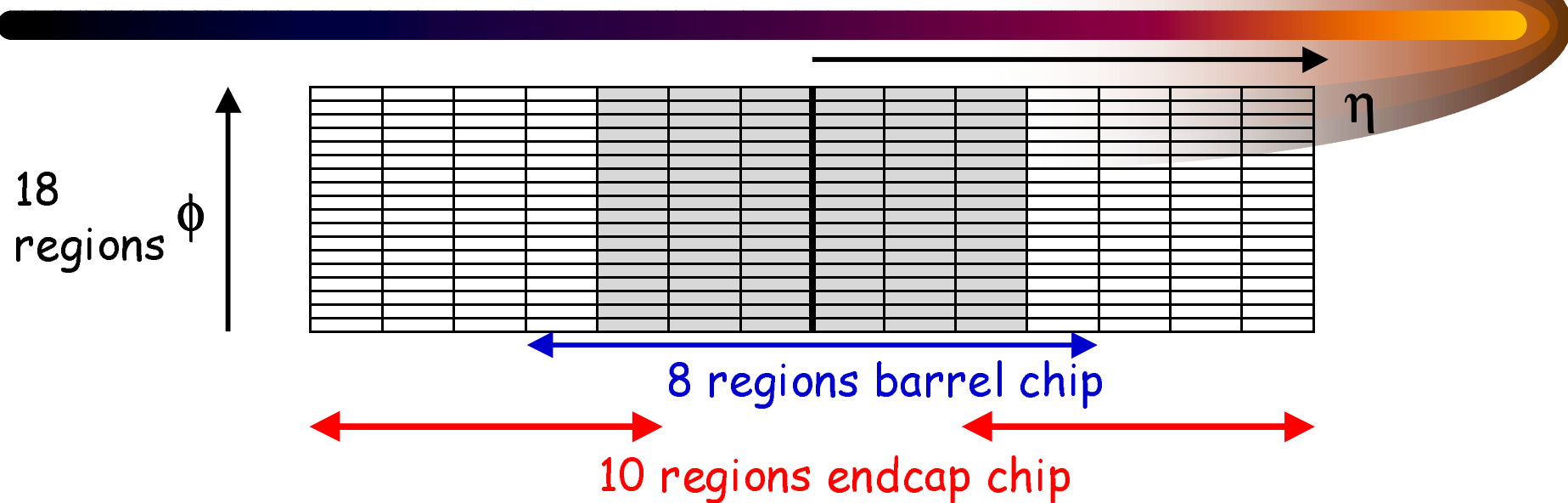
- ⇒ **η -quality modifier** to mark muon as very-low quality (not for use in single muon trigger)

MIP & ISO assignment unit

- Projection logic now included in **MIP & ISO bit Assignment FPGA** (Virtex XC2V3000)
 - 6+6 VirtexII SelectRAM blocks / muon (=96 blocks)
- Project in η and ϕ , separately

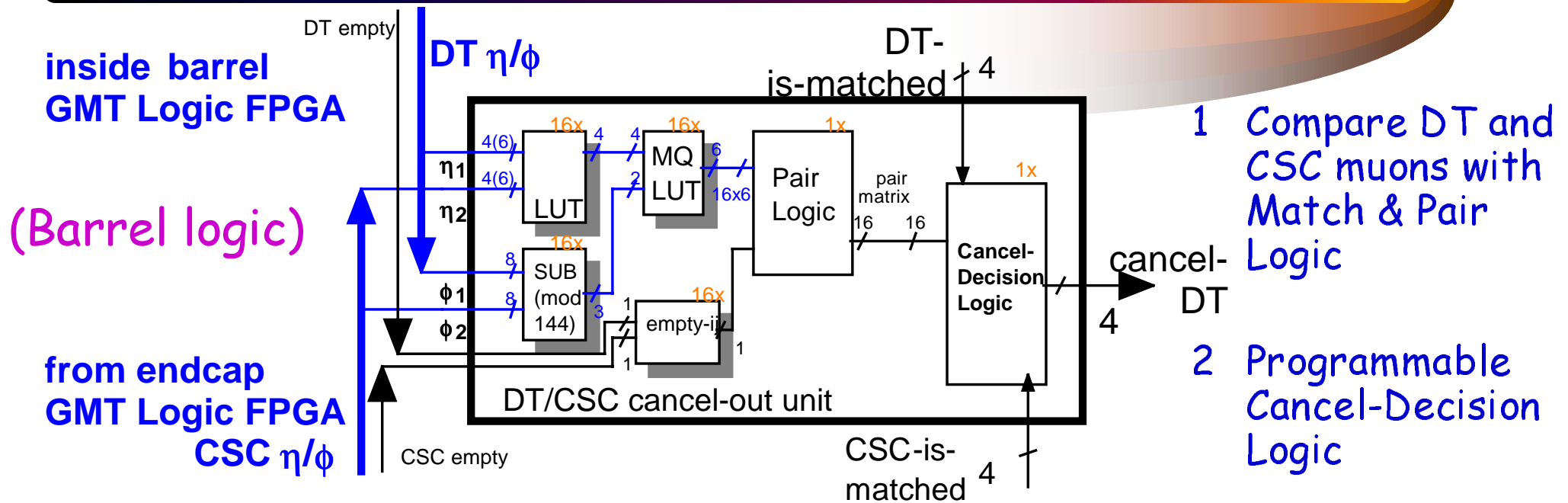


MIP & ISO assignment unit

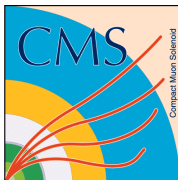


- Different projection for MIP & ISO
 - MIP: project to calorimeter (HCAL in)
 - ISO: project to vertex (jet axis is not bent)
- Different region selection for MIP & ISO
 - MIP: **or** of multiple regions (usually only 1 region)
 - ISO: **and** of multiple quiet regions

New: DT/CSC cancel-out unit



- Current default behavior in case of duplication:
 - cancel the muon (DT or CSC) which is **not** matched with an RPC muon
 - if neither the DT nor the CSC muon is matched with an RPC muon
 - ⇒ cancel the CSC muon
 - if both the DT and the CSC muon are confirmed by an RPC muon
 - ⇒ no cancellation



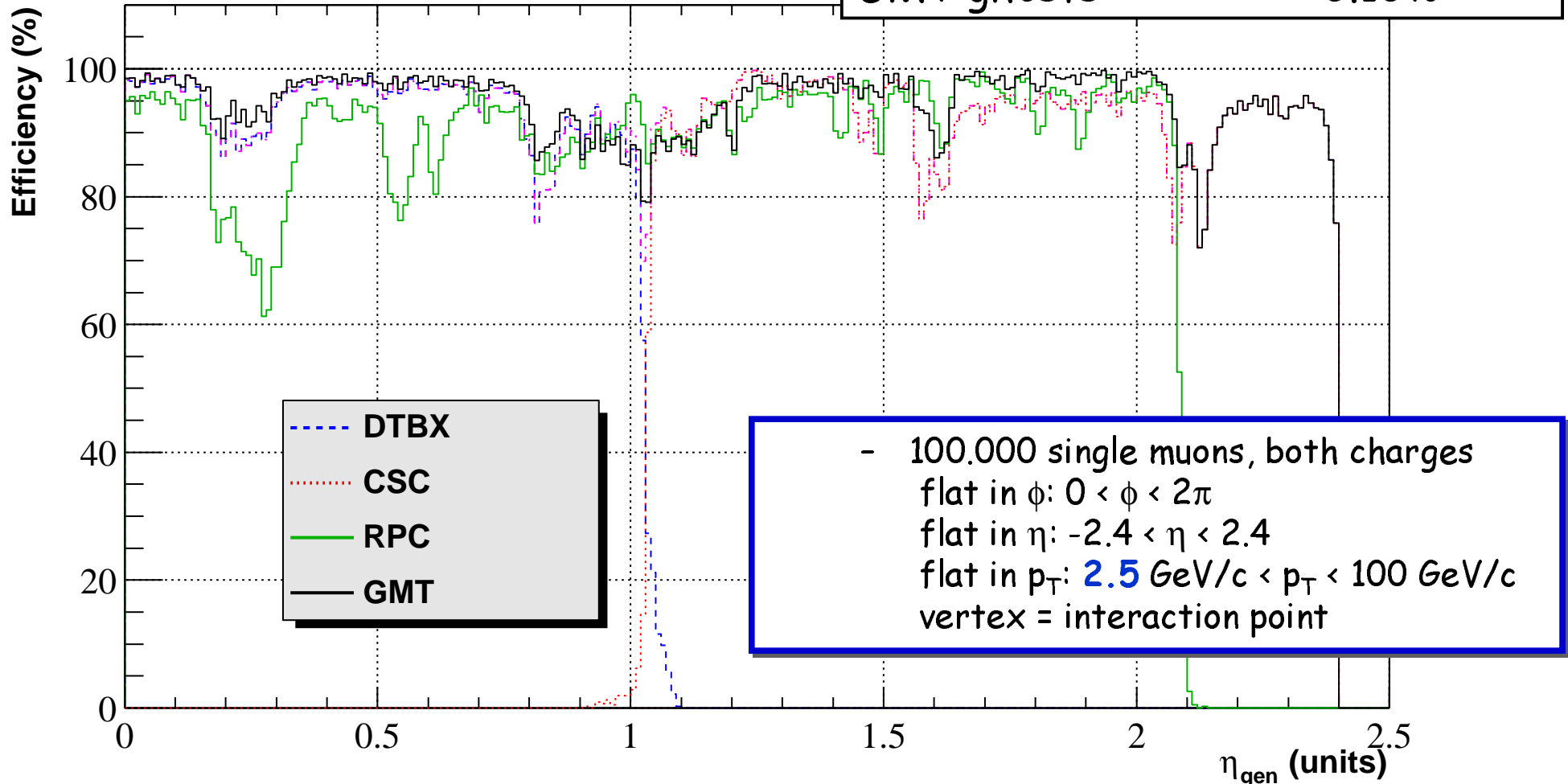
Simulation



- **Software updates** (to be released within ~1 week)
 - new class `L1MuGMTMipIsoAU`
 - new class `L1MuGMTCancelOutUnit`
 - selection: **AND** with RPC in overlap region will be removed
 - match quality calculation adapted to hardware
 - 3 bits $\Delta\phi$, 4 bits $\Delta\eta$, 6 bits match quality
 - matching windows made smaller
 - no change in efficiency, slightly less ghosts: 0.13% \rightarrow 0.10%
 - new GMT output quality to GT defined (3 bits, preliminary)
- **Software update** (to be released within ~1-2 months)
 - re-tuning of selection logic to reduce RPC noise
 - when new MB samples are available \Rightarrow see talk by G. Bruno

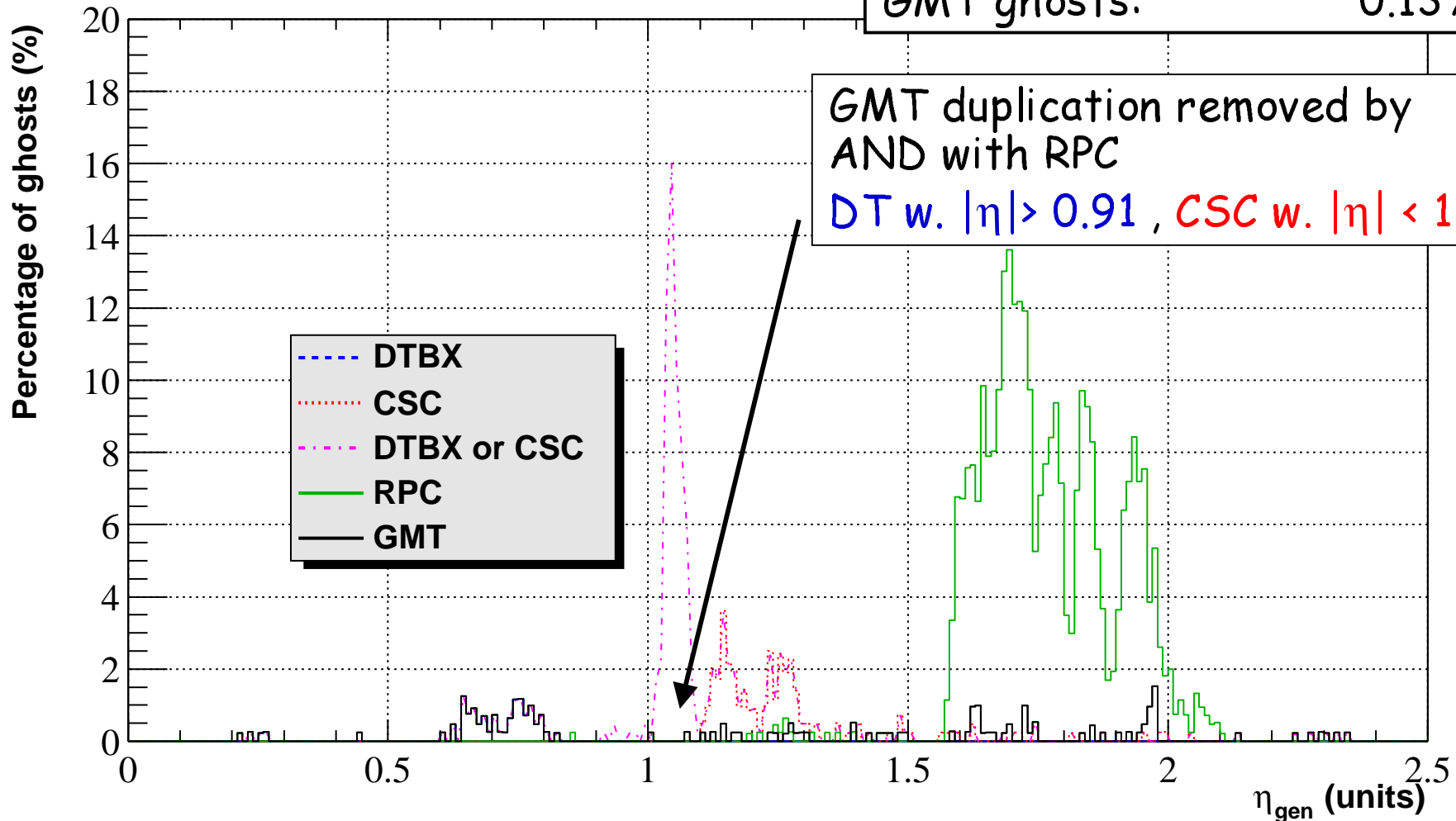
RPC efficiency=0.95

GMT efficiency:	94.80%
GMT ghosts:	0.13%



RPC efficiency=0.95

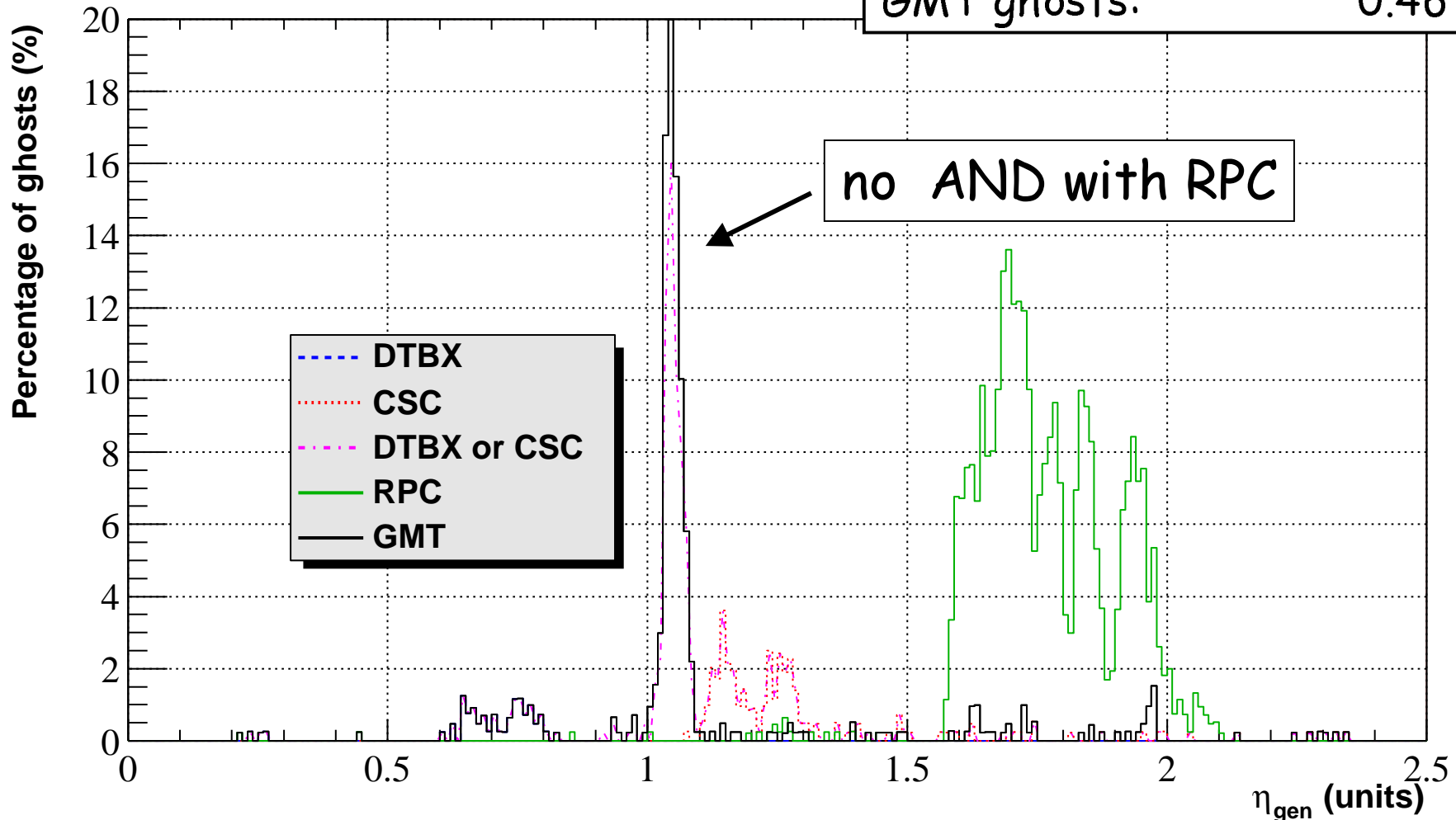
GMT efficiency:	94.80%
GMT ghosts:	0.13%



GMT ghosts vs. η ORCA 4.5.0, CMS 121

RPC efficiency=0.95

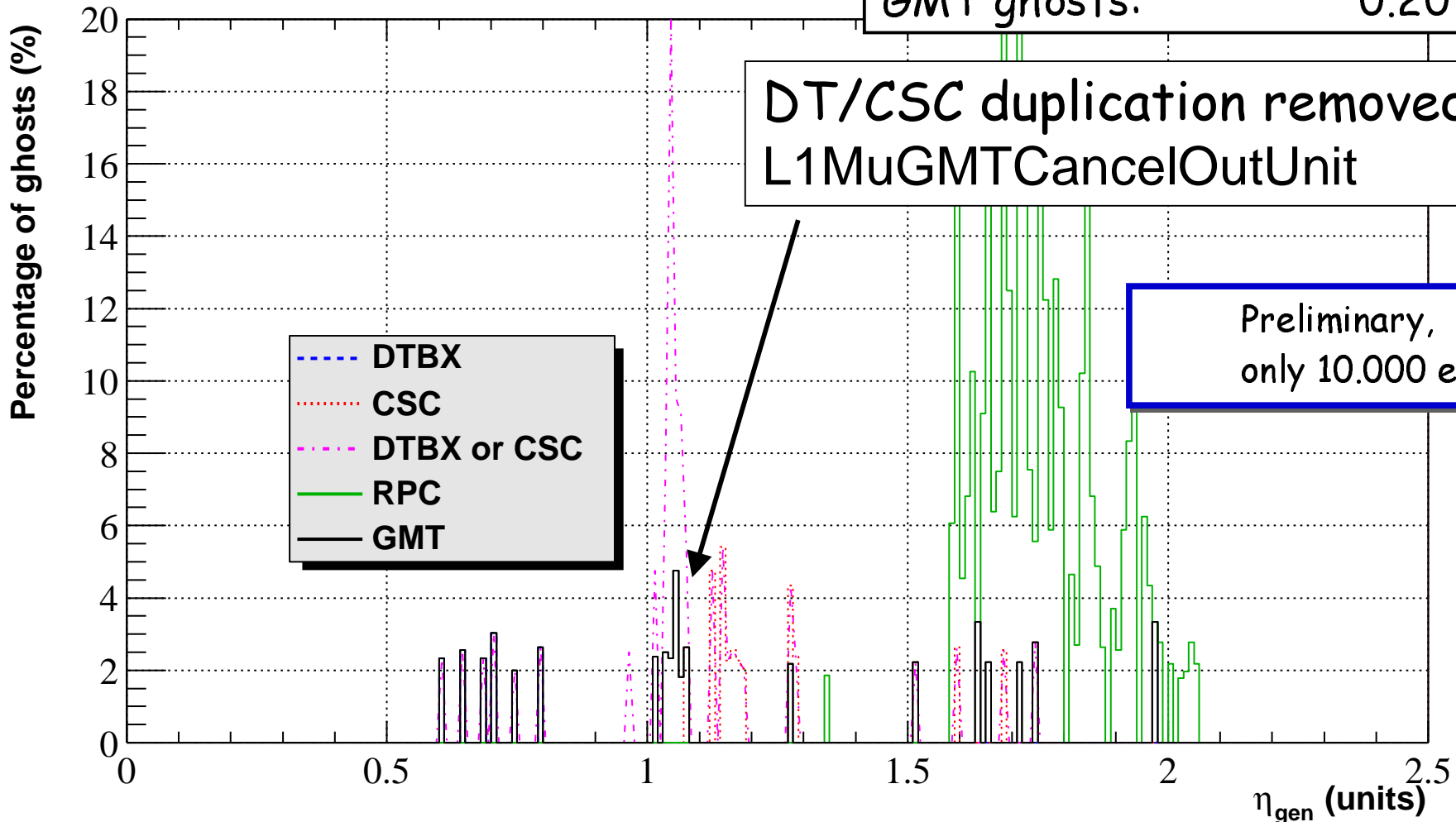
GMT efficiency:	95.23%
GMT ghosts:	0.46%



GMT ghosts vs. η ORCA 4.5.0, CMS 121

RPC efficiency=0.95

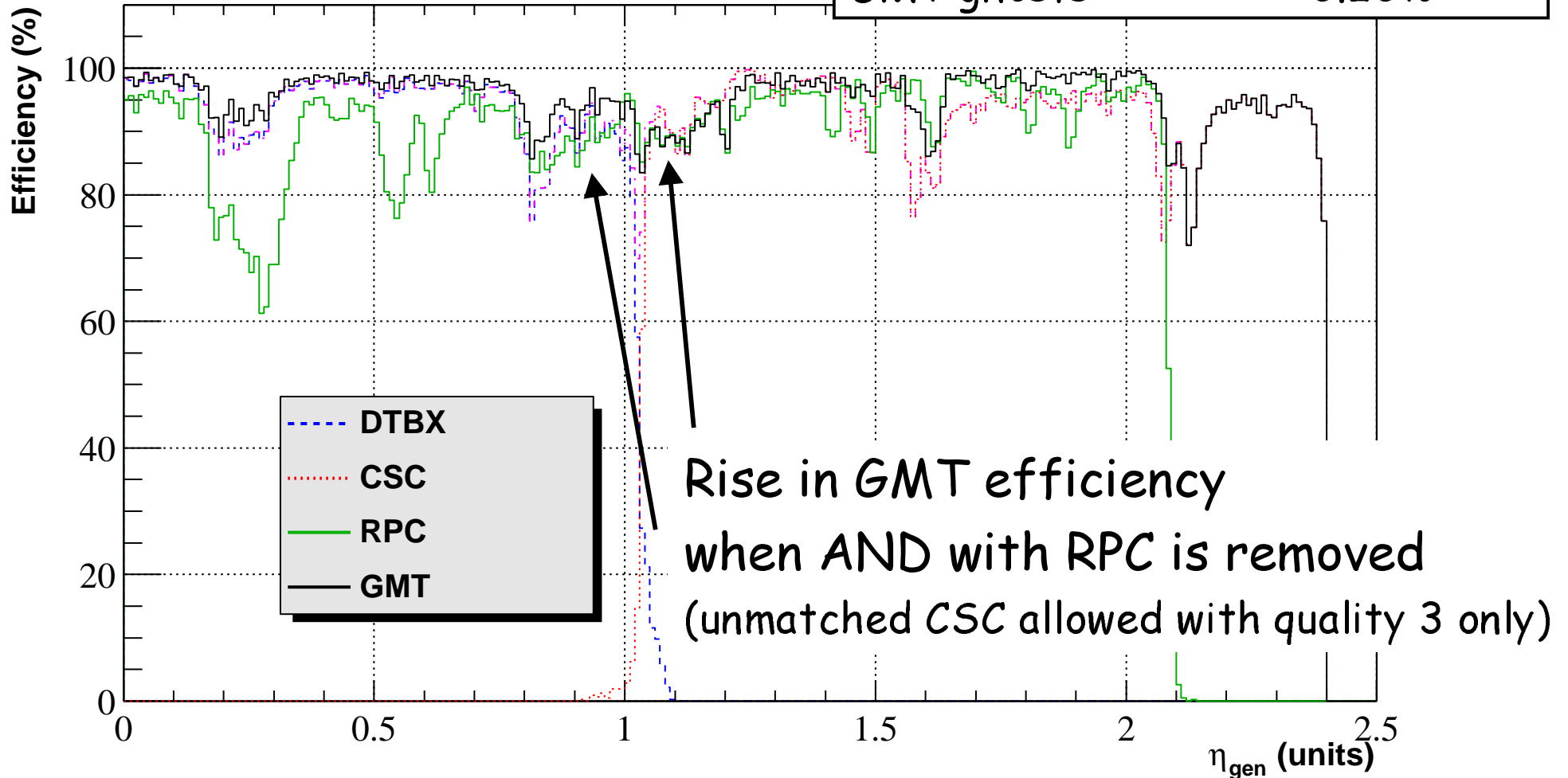
GMT efficiency:	95.33%
GMT ghosts:	0.20%



GMT efficiency vs. η ORCA 4.5.0, CMS 121

RPC efficiency=0.95

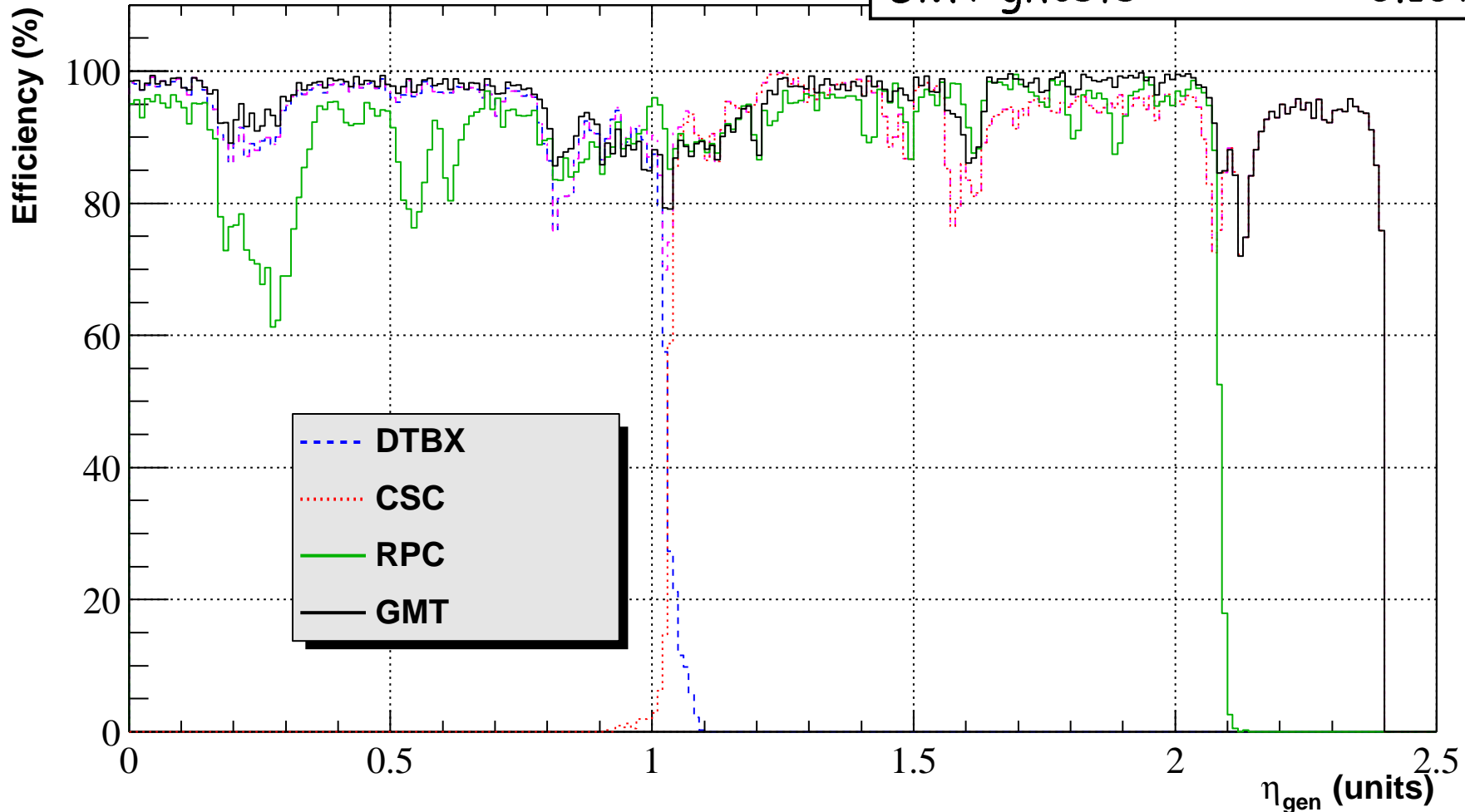
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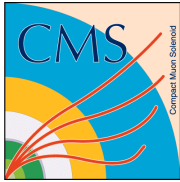
GMT output quality



- Proposed quality coding GMT to GT (3 bits)

q	match	pTsimilar	isDT/CSC	meaning
7	1	1	1	matched, pT taken from DT/CSC, pT measurements agree
6	1	1	0	matched, pT taken from RPC, pT measurements agree
5	1	0	1	<i>matched, pT taken from DT/CSC, pT measurements disagree</i>
4	1	0	0	<i>matched, pT taken from RPC, pT measurements disagree</i>
3	0	1	1	unmatched, DT or CSC
2	0	1	0	unmatched, RPC
1	0	0	1	unmatched muon of very low quality, not to be used in single muon trigger
0	0	0	0	empty channel

if pT-similar information does not prove to be useful, qualities 4 and 5 can be used to give more information about the quality of unmatched muons



Conclusions



- Hardware

- Logic design has been further elaborated (pin counts, chip types, RAM blocks)
- Design has been simplified (no more external RAM for LUTs)
- Ready for VHDL simulation
- Interface documents available as drafts
 - GT web page: <http://sungraz.cern.ch/CMS/trigger/globalTrigger/Welcome.html>

- Simulation

- works in ORCA 4.5.0
- updates to come soon:
 - **new** DT/CSC cancel-out unit
 - MIP & ISO bit assignment now includes muon propagation
 - matching optimized (windows smaller)
- Study on effect of RPC noise & GMT \Rightarrow *see talk by G. Bruno*
- Study on MIP & ISO bit assignment \Rightarrow *see talk by N. Amapane*