

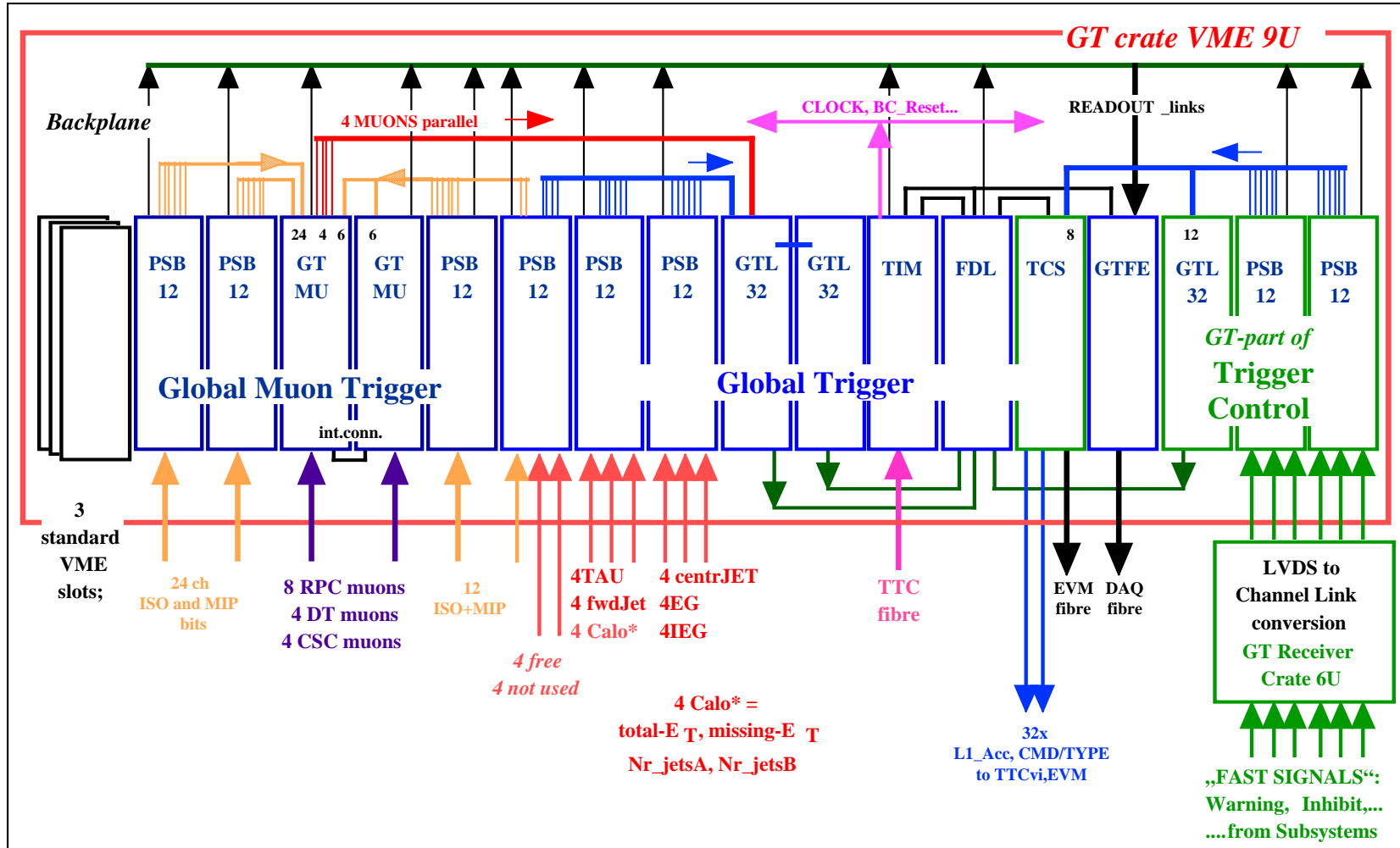
Global Muon Trigger

Conceptual Design

N. Neumeister, H.Sakulin, A.Taurok

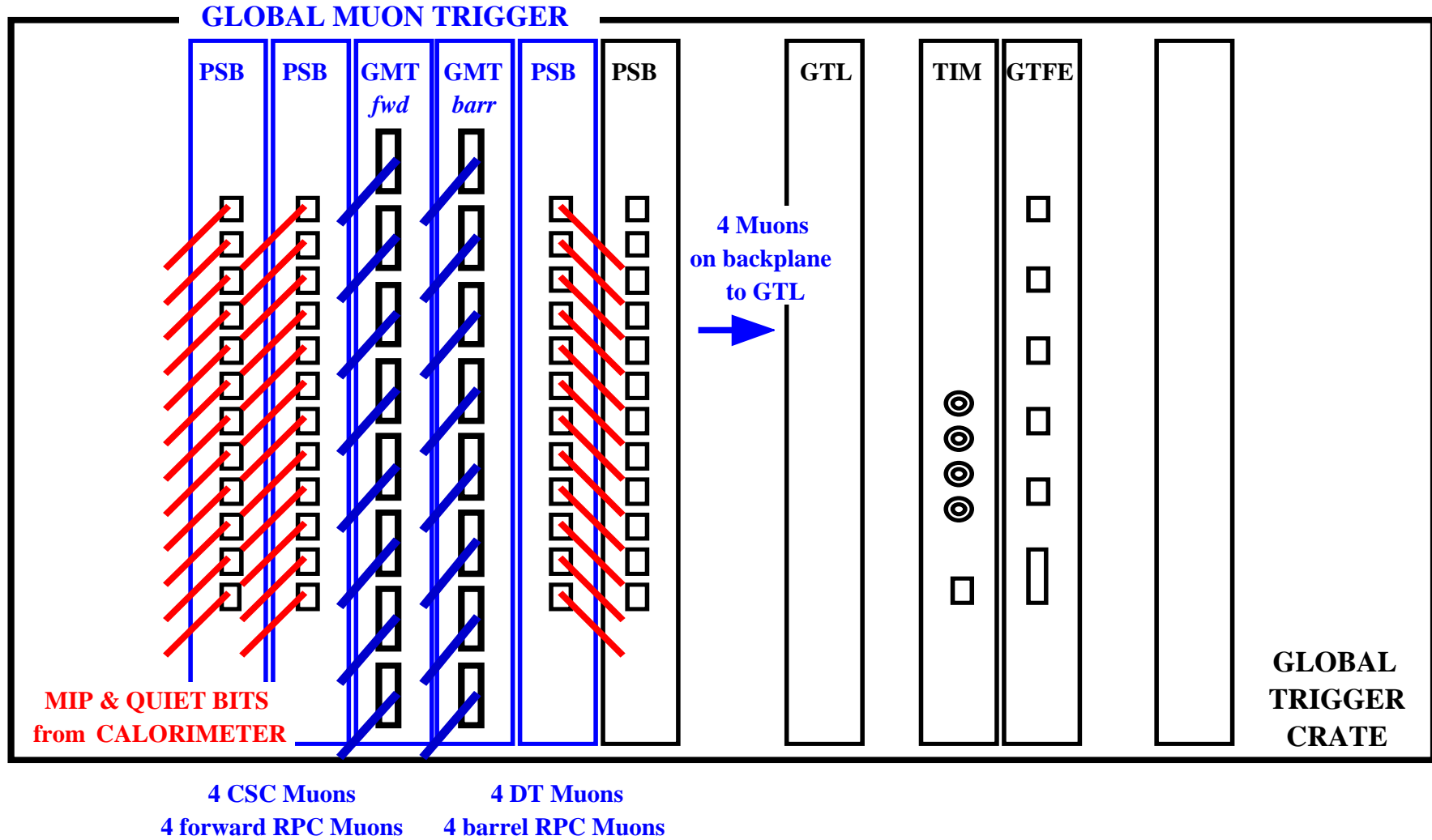
Trigger meeting, TRIDAS Week,
6. Nov 2000, CERN

Global Trigger Crate





GMT in GT Crate

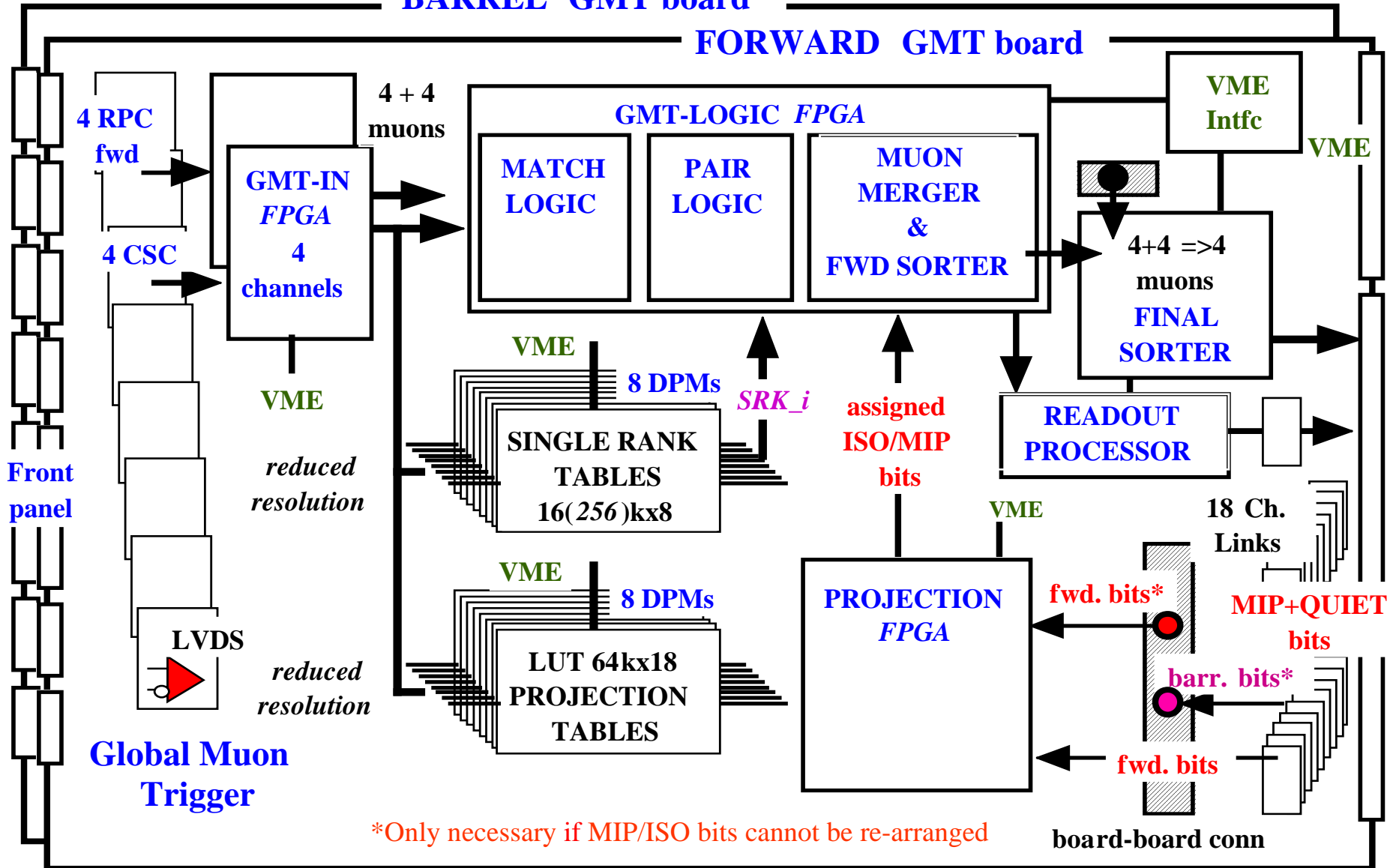




GMT Logic Boards

BARREL GMT board

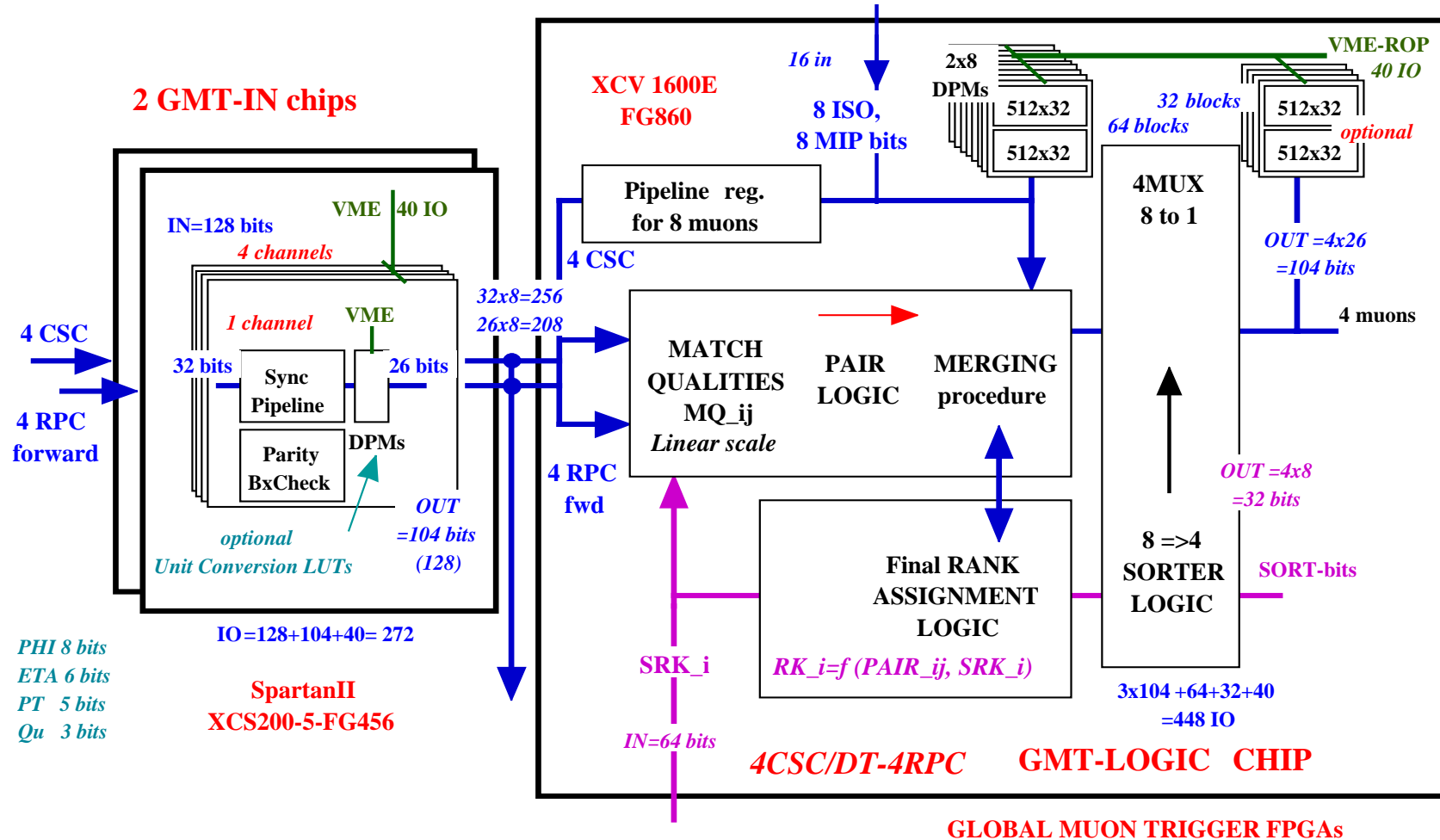
FORWARD GMT board



*Only necessary if MIP/ISO bits cannot be re-arranged

board-board conn

GMT Input and Logic FPGA





Matching Logic



- **Unit conversion for η and ϕ .**
- **For all possible pairs 16 differences are calculated:**
 - $\Delta\eta_{ij}$, $\Delta\phi_{ij}$, ...*4 bit numbers for small differences*
 - *subtractor for ϕ*
 - *optional subtracting LUT for η*
- **16 lookup tables 256 x 6 bits \Rightarrow 16 MATCH QUALITIES**
 - $MQ_{ij} = f(\Delta\eta_{ij}, \Delta\phi_{ij})$
 - **High match quality \Leftrightarrow both muons are close in space**



PAIR LOGIC

16 Match Qualities for all possible pairs generated using LUTs.

48 COMPARATORS: compares Match Qualities of all possible pairs to each other

6 comp's per hor. line and 6 per vert. row:

GE11_12, GE11_13, GE11_14, GE12_13, GE12_14, GE13_14

GEij_kl = MQ_ij >= MQ_kl

GEij_kl = / GEkl_ij

pt_ij = pt_i > 0 + pt_j > 0

mq_ij = MQ_ij > 0

// INVERTED VALUE to get one best match per line

// one pt has to be >0

// Match quality above min. value

MAX matrix: For each pair calculate if it has a better match quality than its 3 horizontal and 3 vertical neighbours.

*MAX_11 = GE11_12 * GE11_13 * GE11_14 * GE11_21 * GE11_31 * GE11_41 * pt_11 * mq_11*

*MAX_12 = /GE11_12 * GE12_13 * GE12_14 * GE12_22 * GE12_32 * GE12_42 * pt_12 * mq_12*

etc.

16 AND6 functions

DIS matrix: Each pair can be disabled by MAX bits from its 3 horizontal and 3 vertical neighbours.

In other words: Each MAX_ij goes to its 3 hor. and 3 vert. neighbours to disable them.

DIS_11 = MAX_12 + MAX_13 + MAX_14 + MAX_21 + MAX_31 + MAX_41

DIS_12 = /MAX_11 + MAX_13 + MAX_14 + MAX_22 + MAX_32 + MAX_42

etc.

16 OR6 functions

PAIR matrix: =1...The match quality of the pair is better than the MQ of the 6 neighbours, which are not disabled by a MAX_ij bit.

*PAIR_11 = (GE11_12 + DIS_12) * (GE11_13 + DIS_13) * (GE11_14 + DIS_14) **

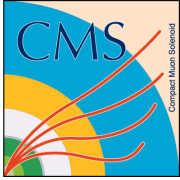
*(GE11_21 + DIS_21) * (GE11_31 + DIS_31) * (GE11_41 + DIS_41) * pt_11 * mq_11*

*PAIR_12 = (/GE11_12 + DIS_11) * (GE12_13 + DIS_13) * (GE12_14 + DIS_14) **

*(GE12_22 + DIS_22) * (GE12_32 + DIS_32) * (GE12_42 + DIS_42) * pt_12 * mq_12*

etc.

16 OR-AND functions



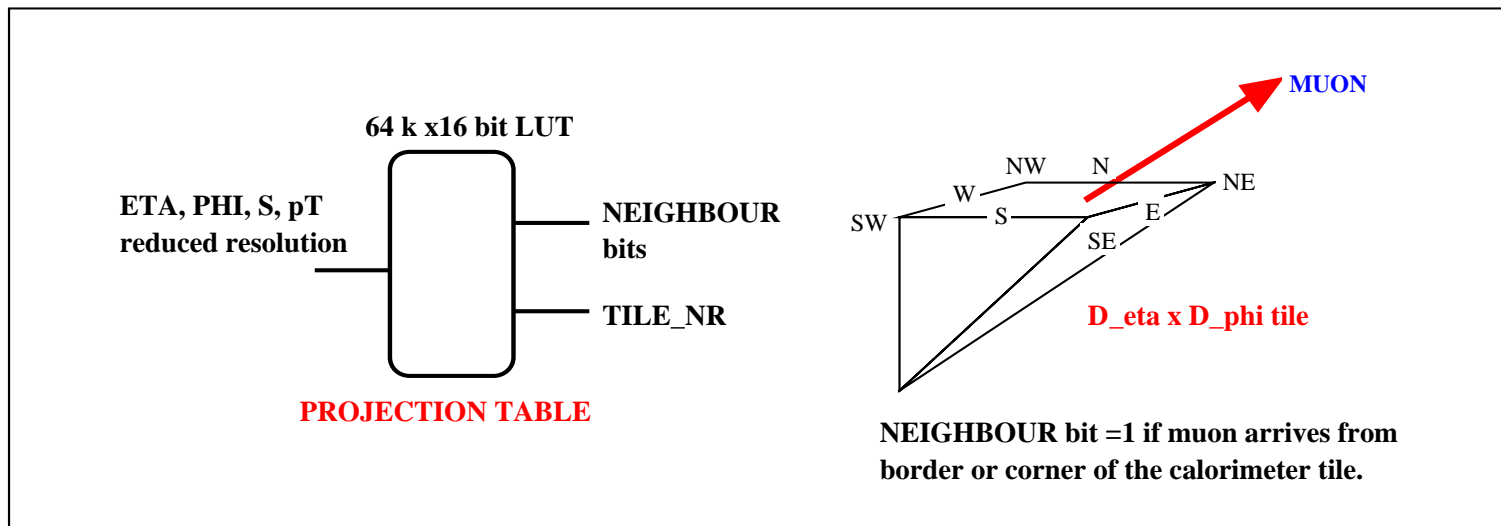
Merging Logic



- ***Optional procedures:***
 - **winner/loser implementation**
 - ...takes “better” candidate of a matched muon pair.
 - *The Single ranks of both muons are compared to decide between both muons*
 - **parameter selection implementation**
 - takes the “best” measured items (ϕ , η , p_T , charge) from both muons.
 - **parameter mixing implementation**
 - calculates a new coordinate or p_T
 - **Current GMT- ORCA simulation (ORCA 4.3.0) uses**
 - the winner/loser method for η , ϕ and charge
 - parameter mixing for p_T to obtain minimum p_T

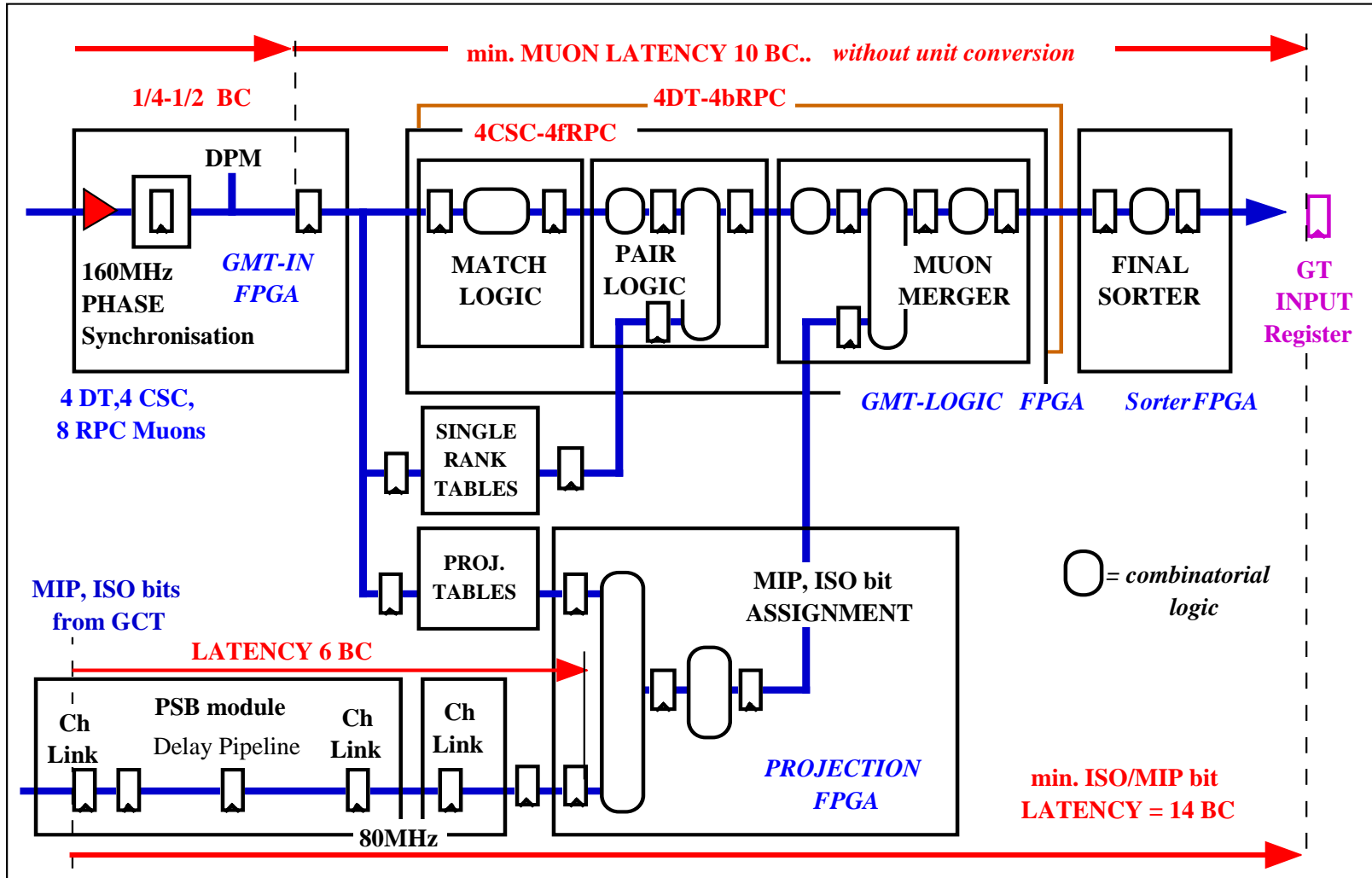
MIP and ISOLATION Bit Assignment

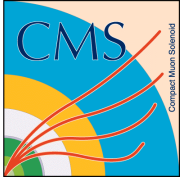
- **Rearrangement of MIP and QUIET bits** \Rightarrow **no board-to-board connector**
 - 18 Barrel cables: $\eta = -3\dots+3 \Rightarrow 8$ QUIET + 8 MIP bits = 16 bits/ $\Delta\phi$ wedge
 - 18 Endcap cables: $\eta = -6\dots-2, +2\dots+6 \Rightarrow 10$ QUIET + 10 MIP bits = 20 bits/ $\Delta\phi$ wedge
- **Projection tables for each muon**



- **PROJECTION FPGA assigns MIP and ISOLATION bit**
 - Combinatorial logic finds out, if the QUIET and MIP bits are set corresponding to the tile number of the muon. The logic for each muon consists of two 8-to-252 bit decoders, a number of 'and-or' gates and two or252 gates.

Estimated GMT Latency





Plans for 2000 - 2004



- Nov 2000 writing CMS note on conceptual design
- 2001 Simulation and start design of FPGA chips
- 2002 Design of FPGA chips
- 2003 production of VME 9U boards
- 2004/2005 production of spare modules



Milestones 1999-2004

- **D431 - June 1999**
 - *PSB_6U prototype production* *Status: **Board tested.***
 - *BACK6U design* *Status: **done***
- **D432 – Nov 1999** *milestone changed*
 - *BACK6U production* *Status: **Board in use.***
- **D433 - June 2000**
 - *GTL_6U design* *Status: **Delay due to redesign***
- **D434 – Nov 2000** **Trigger Logic Functions tested**
 - *GTL_6U tested;* *Status: **Delay***
 - *FDL_9U design* *Status: **Delay***
 - *Combined logic test: Backplane + PSB + GTL* *Status: **Delay***
 - *Conceptual Global Muon Trigger design* *Status: **done , ..merging logic***
- **D435 - Nov 2001** **Complete Logic Pipeline tested**
 - *Combined Prototype test: Backplane + PSB + GTL+FDL*
- **D436 - June 2003** **24-channel Global Trigger available**
- **D437- Nov 2003** **Global Muon Trigger available**
- **D438 - Nov 2004** **32-channel Global Trigger available**