CMS Global Muon Trigger Update

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URL of this presentation:

Rack S1-E04
CMS Level-1 Trigger

Calorimeter Trigger

HF → HCAL → ECAL → Regional Calorimeter Trigger → Global Calorimeter Trigger

Muon Trigger

RPC → CSC local trigger → CSC Track Finder → Global Muon Trigger

DT → DT local trigger → DT Track Finder → Global Muon Trigger

Pattern comparator trigger

MIP+ ISO bits

e, j, E_T, H_T, E_T^{miss}

4+4 μ, 4 μ, 4 μ

4 μ (with MIP/ISO bits)

L1 Global Trigger

Pipelined 40 MHz, Latency < 3.2 μs

max. 100 kHz

L1 Accept

CMS Global Muon Trigger Update
Global Muon Trigger Overview

252 MIP bits
252 Quiet bits

4 µ RPC brl

4 µ DT

4 µ CSC

4 µ RPC fwd

Inputs:
8 bit $\phi$, 6 bit $\eta$, 5 bit $p_T$, 2 bits charge, 3 bit quality, 1 bit halo/$\eta$ fine-coarse

Output:
8 bit $\phi$, 6 bit $\eta$, 5 bit $p_T$, 2 bits charge/synch, 3 bit quality, MIP bit, Isolation bit
Global Muon Trigger Tasks

- Synchronizing
- Matching & Pairing DT & brlRPC, CSC & fwdRPC
- Merging parameters
- Converting scales ($\eta$)
- Detecting ghosts, fake triggers
- Canceling out duplicated candidates in the overlap region
- Propagating to calo/vertex for MIP/Iso bit assignment
- Ranking & Sorting
GMT in the Global Trigger Crate

1 GMT Logic Board

FPGA firmware ready

3 Pipeline Sync. Boards

6-channel prototype available

Special wide input board parallel to front panel

Global Trigger Crate
(top view)

4 DT/CSC + 8 RPC muons

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CMS Global Muon Trigger Update
GMT Logic Board

PCB received last week

M. Padrta
GMT Logic Board

Connectors to input board

4 SCSI connectors on Logic Board
3x4 on input board

Input fwdRPC
Input CSC
Input DT
Input brlRPC
MIP/ISO fwd
MIP/ISO brl
SORT
ROP

M. Padrta
GMT Logic Board

Connectors to input board

4 SCSI connectors on Logic Board

3x4 on input board

Input fwdRPC
XC2V1500
FF896

Input CSC
XC2V1500
FF896

Input DT
XC2V1500
FF896

Input brlRPC
XC2V1500
FF896

Logic fwd
XC2V3000
BF957

Logic brl
XC2V3000
BF957

MIP/ISO fwd
XC2V3000
BF957

MIP/ISO brl
XC2V3000
BF957

SORT
XC2V2000
BF957

ROP
XC2V2000
BF957

VME64

4 SCSI connectors on Logic Board

3x4 on input board

M. Padra
GMT Input Board

PCB expected this week

Mounted in Parallel to front panel of crate.
Connectors for 2\textsuperscript{nd} 3\textsuperscript{rd} and 4\textsuperscript{th} muon
from DT, CSC, barrel RPC, forward RPC

Layout and routing finished.
Production this month.

M. Padrta
Mezzanine BF957

- For 6 chips on GMT Logic Board
  - Logic FPGAs
  - MIP/ISO Assignment FPGA
  - Sort FPGA
  - ROP

Available. Currently mounting connectors

A. Taurok, M. Padrta
Plans until the end of the year...

- Assemble the GMT Logic Board, Mezzanines, Input Board
- Test
  - Connection Tests
  - Internal self-test
    - Generate Data in Input FPGAs, spy it with Sort FPGA
  - Interconnection tests
- Develop online software at same time
  - Use the same framework (VME64 board configuration, …) as for GT
Not yet with GMT Logic board

Instead: Final Decision Logic (FDL) board of Global Trigger

- Same VME64 interface chip as on GMT
- Same JTAG Controller firmware (developed by J. Ero) as in GMT ROP

The test

- Access the JTAG chain on the FDL board
- Try to load firmware into PROMs

Hardware used

- JTAG Controller Firmware
- VME64 Chip (Altera)
- SBS VME Interface

Software used

- Hardware Access Library (HAL)
- JTAG Access Library (JAL)
- Command Line utility
(Pre-)Test: VME-JTAG

- Successfully verified and upgraded FDL firmware (Xilinx XC18V04 PROMs)

VME64 chip (Altera)
SBS PCI-VME
JTAG Controller Firmware
JTAG Chain
Xilinx XC18V04

Command line utility

Firmware (Serial vector format)

SVF file

JTAG Access Library
Hardware Access Library

hardware

Xilinx IMPACT

VME64 chip (Altera)
SBS PCI-VME
JTAG Controller Firmware
JTAG Chain
Xilinx XC18V04

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CMS Global Muon Trigger Update
GMT consists of
- 3 pipeline synchronizing boards … prototype available
- 1 GMT logic board + front panel … PCB received, starting to assemble

FPGA design for GMT logic board in progress
- Input FPGA (4x) … firmware completed
- MIP and ISO assignment unit (2x) … firmware completed (brl+fwd)
- GMT logic FPGA (2x) … firmware completed (brl+fwd)
- Sorter FPGA (1x) … firmware completed
- ROP Chip (1x) … firmware completed

Milestones
- (Dec 01) Dec 02: logic design completed … completed
- (Dec 02) Dec 03: FPGA design done … completed
- (Dec 03) Dec 04: Board Prod. Done … making progress
- (Jan 04) Dec 04: GMT integration tests start … making progress
- (Jun 04) Feb 05: GMT tested … making progress
- (Jan 05) Feb 05: GMT integration tests completed … making progress
Summary

- GMT Logic Board: received PCBs
  - Starting assembly & tests

- Firmware of all ten FPGAs completed
  - 100% agreement between firmware and ORCA (C++) simulation

- Pre-tests started
  - Successfully upgraded firmware via JAL / HAL / VME / JTAG in similar configuration

- Development of on-line software started
  - JTAG Access Library (JAL) now complete
  - Tested with FDL board
  - Also tested with CSC Sector Processor board

... see talk this afternoon