

CMS Internal Note

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PHASE SYNCHRONISATION of trigger data in the CMS Level 1 Global Trigger

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Abstract:

A digital circuit is described to synchronise the phase of Level 1 trigger data from different detectors to the local 40 MHz clock of the Level 1 Global Trigger. It is used as the input stage of the bunch crossing synchronisation circuit, which consists either of a programmable pipeline delay or a short FIFO. Limits and constraints of the circuit are described and hints for realisation in FPGA chips are given. It is assumed that all trigger systems are driven by a common clock signal that is distributed by the TTC system[1].

Introduction

In CMS the TTC system sends a common clock signal to all parts of the Level 1 trigger electronics to synchronise it to the bunch crossings of LHC. In every TTCrx [2] clock receiver chip a coarse and a fine delay register shift the phase of the 40 MHz clock. Therefore the phase of input data from an upstream part of the trigger system could be shifted by set-up procedures. In case of cables with an optimised length then the phase of the local clock would have to be adjusted too to take the data correctly. But this solution fails if trigger data arrive from trigger parts controlled by different TTCrx chips. Then the phases of all input channels have to be synchronised to the local 40 MHz clock. Monitoring circuits have to watch the input channels continuously to see any changes in phase either due to a set-up procedure or due to a hardware failure.

The L1 Global Trigger receives trigger data from the Global Calorimeter Trigger and the Global Muon Trigger [3]. It has to synchronise all channels in phase and in bunch crossings (=bx) to each other and to combine data from the same bunch crossing.

Phase Synchronisation of input data

Instead of using programmable delays all data bits are over-sampled with 160 MHz and the best sample is selected and fed into the following pipeline logic. Of course for one of the samples the set-up/hold conditions will be violated but this sample must never be selected.

In the L1 Global Trigger on the PSB boards [3, 4] where the input channels are synchronised to each other a PLL circuit generates a local 80 MHz clock signal (=CLK80) from the 40 MHz clock (=CLK40). Both clock signals are distributed on the board and inside the FPGA chips with a time skew smaller than the switching time of the FPGA flip-flops.

Each bit of the input channels is sampled 4 times per bunch crossing period at the rising and falling edges of CLK80 to get a 160 MHz sampling rate. Then the best of the four samples is selected and transferred to the following 40 MHz pipeline logic. See Fig.1.

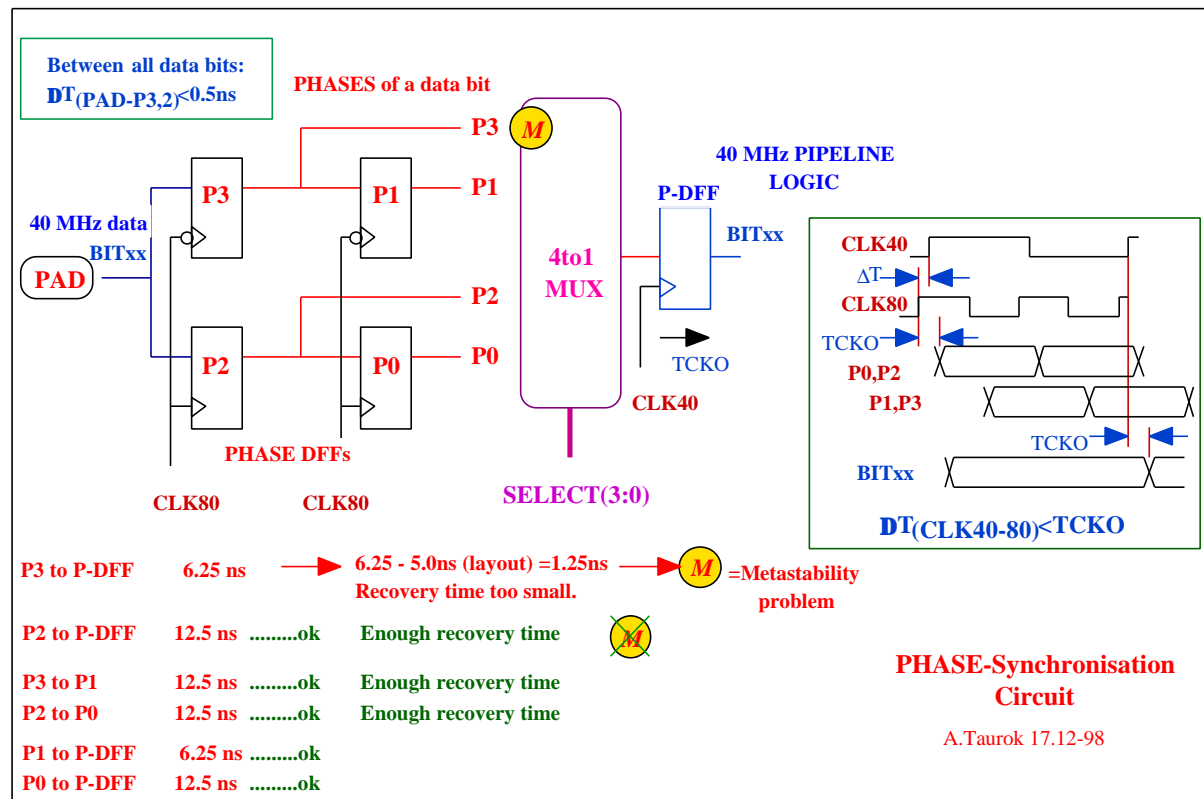


Fig.1 Phase Synchronisation circuit

Timing conditions

See Fig. 2 and 3.

All data bits and both clock signals have to meet the following time constraints:

SMALL SKEW ($<2.1\text{ns}$) between bits of one channel relative to CLK80

→ Data bits of one channel come from one Receiver chip (skew $<1\text{ns}$)

→ Board layout: Similar net length (skew_bits $<0.4\text{ns}$)

→ Layout of SYNC chip (skew_clock80 <0.2 + skew_bits $<0.5\text{ns}$)

SMALL SKEW ($<1.2\text{ns}$) between CLK80 and CLK40 at each data bit

→ 40 & 80 MHz CLK locked by Clock chip (skew_clk2clk $<0.5\text{ns}$)

→ Board layout: Equal net length for CLK40 and CLK80 $<0.2\text{ns}$

→ FPGA layout: difference between CLK40 and CLK80 $<0.5\text{ns}$

Remark: CLK80 goes to less DFFs, therefore the delay inside the FPGA is smaller than for CLK40. The Clock control chip should compensate the difference.

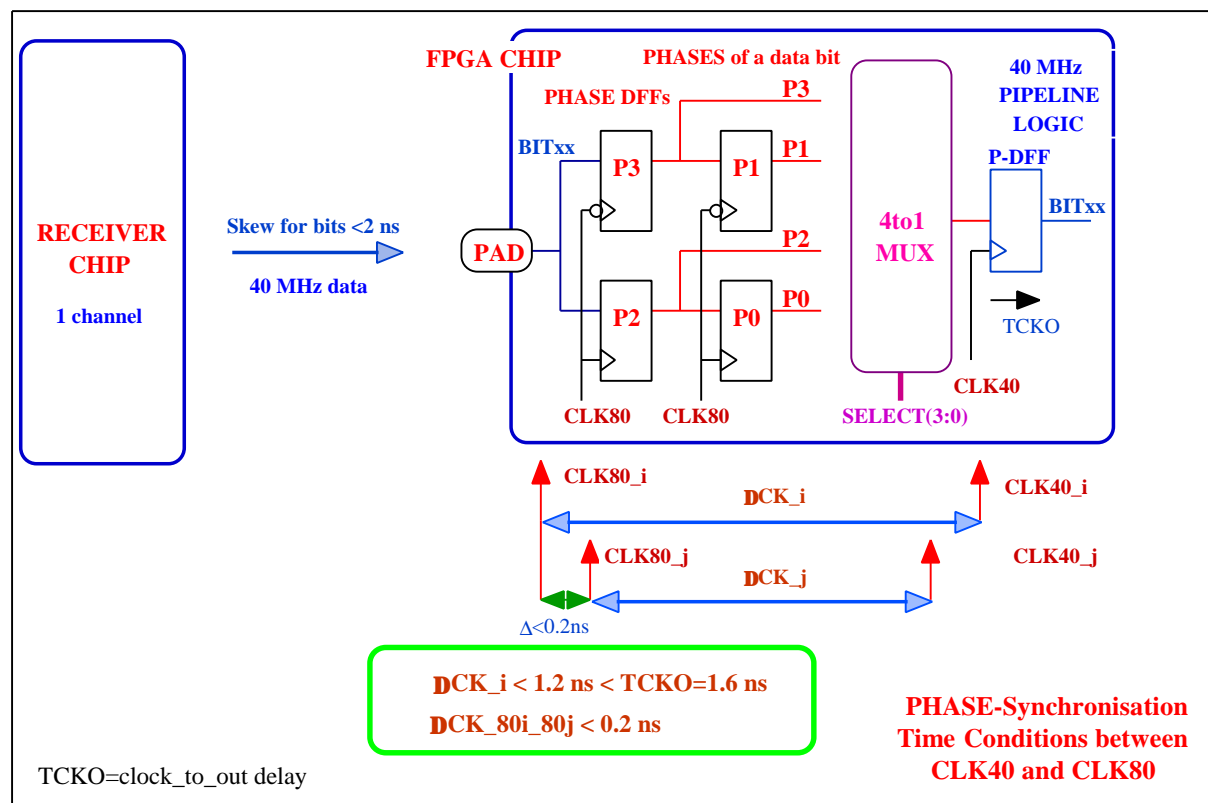


Fig.2 Time conditions between CLK40 and CLK80

FPGA Layout of phase circuit:

Example: XILINX 40xxXL-1

Each input data bit goes to two phase DFFs (DFF=data flip-flop). One DFF stores the data bit at the rising edge of the 80 MHz clock and the other DFF at the falling edge. At the next CLK80 tick both values are shifted to the next two phase DFFs to get 4 samples per one CLK40 tick.

Both first phase DFFs P3 and P2 are placed next to the input pad into the same CLB (Configurable Logic Block) to guarantee for the data bit the same short net length from the input pin to both phase DFFs P3 and P2. The following DFFs P1 and P0 are placed into the next CLB. In the 3rd CLB a 4-to-1 Multiplexer switches then one of the samples to the first

DFF of the following 40 MHz pipeline logic. The layout of the phase logic was done manually to achieve the necessary short delays and a small skew for all bits. Very strict time constraints have to be respected to get a reliable design. The CLK80 should arrive within <0.5 ns (prototype design <0.13 ns) at all phase DFFs of all data bits of one channel and the net lengths from the input pads for all bits should vary only within <0.5 ns. Both conditions are necessary to sample all input data bits at the same time. For every data bit the CLK40 should arrive at the following pipeline logic at the same time ($\Delta t < 1\text{ns}$) as CLK80 at the phase DFFs to store the selected phase correctly. The time difference has to be smaller than the clock-to-out switching time of the DFFs [$\Delta t(\text{clk40-clk80}) < t_{\text{cko}} = 1.6\text{ns}$ for XC4k_xl-1]. Low skew global nets were used for the clock distribution.

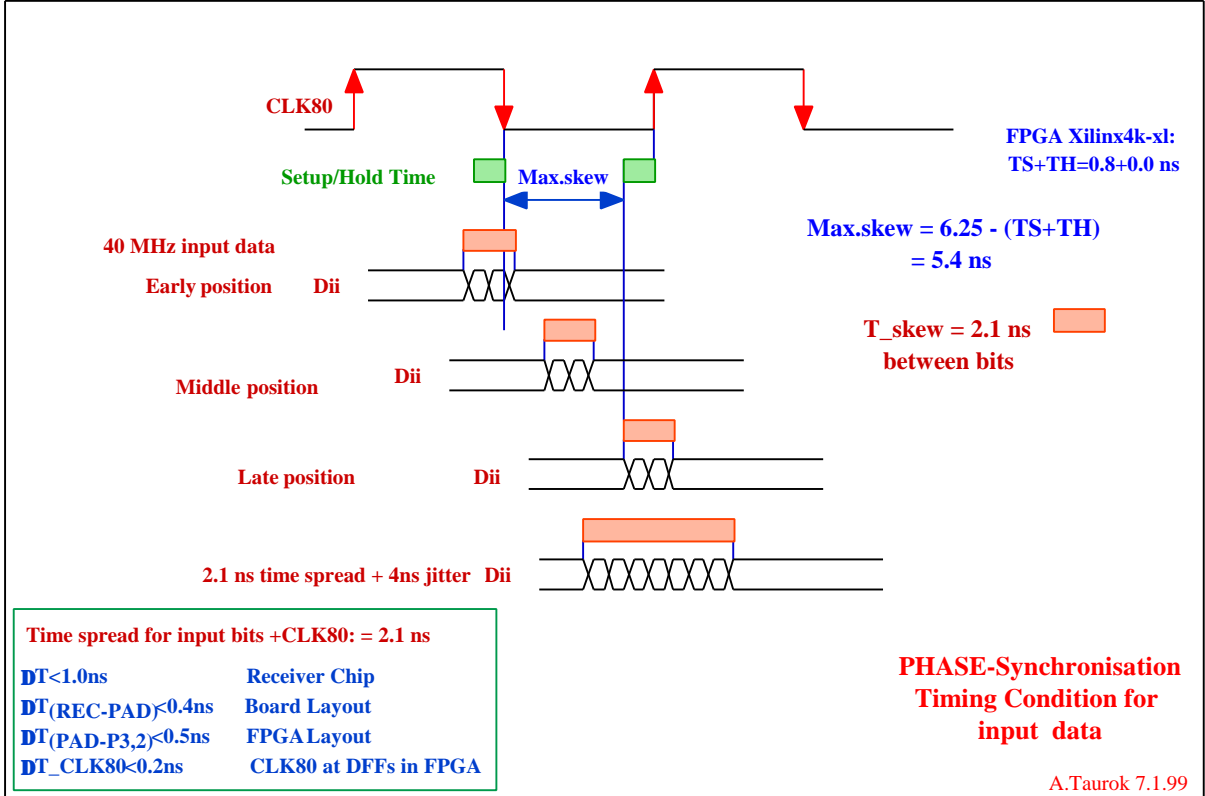


Fig.3 Timing condition for input data

Violations of Set-up/Hold Time

See Fig.2 and Fig3.

When the input data change their state within the setup/hold period of the phase DFFs P3, P2 then the outputs of P3, P2 could go into a metastable state. The nets and combinatorial logic delays till the following DFFs should be short enough to allow the phase DFFs P3 and P2 to recover. For a design with all delays <5.0ns for the nets P0,1,2,3 the safety margin is long enough to avoid metastability problems except for the P3 to P-DFF path. The recovery time of about 1.25 ns for P3 to P-DFF might be too small. **But the phase where the input bits change their logic state next to the CLK80 edge should never be connected to the pipeline P-DFF. Therefore set-up/hold violations and even metastability problems in P3 will not degrade the reliability of the circuit after a correct adjustment.**

Additional time jitter: See Fig. 3.

In addition to the time spread of the bits a time jitter up to 4 ns increments two consecutive phase-compare counters too (4ns + 2.1 skew < 6.25ns) and cannot be distinguished from simple set-up/hold time violation.

Additional time jitter up to 10 ns increments three phase compare counters. A phase can be selected still. But reliability starts to degrade and the phase-test data should then be checked all the time. Above that limit there is no way to find a reliable phase for input data. It's necessary then to find hardware reasons for such unstable behaviour of the links.

Phase Adjustment Procedures and Monitoring

See Fig.4.

Find and select the best sampling time:

For one bit of a channel all 4 phase samples are saved and added to the bunch crossing data. The same four phase samples are compared to each other (XOR) to detect the switching time of the input data and to increment phase compare counters. Four phase compare counters count the number of input transitions per time interval ($t = n$ LHC cycles). The counter with the maximum content indicates the switching time. If the clock edge violates the set-up/hold time conditions two adjacent phase-compare counters are incremented. Then all data bits change their state around the corresponding clock edge. If data increment one Phase Counter only, then the switching time of all data bits is somewhere between the early and late position in Fig.3.

To minimise the latency time the phase just before the rising edge of CLK40 should be selected (P3) but only when at least one of the phase-compare counters with P3 is zero. If not, then try P2 etc. Considering the time spread of bits the phase most far away from the data transition time should be preferred. That means that both phase-compare counters should be zero for the selected phase. The phase close to the switching time can be used only if test measurements show a very stable time behaviour of the link.

Tests during data taking run:

The phase compare counters are read during data taking runs by the monitoring program and for every bx the phases of one bit are appended to trigger data as bits 28 to 31. For a more precise check phase-test data should be sent and checked during the gap(s) of the LHC orbit.

Fast test before or between data taking runs:

To find the switching time of data more precisely and to check the reliability of the link test-data should be sent and read with different phases selected. All bits should be checked to find excessive time shifts.

Measure the stability of input channels in time:

To measure the stability of an input channel below 6.25 ns the fine delay register in the TTCrx or the phase shifting circuit on the TIM Timing board is used to move the clock phase in small steps (0.1-0.5 ns) and for each delay the phase-compare counters and all test data are read. The reset interval for the counters should be set long enough to accumulate higher statistics. This test should be done during the set-up period.

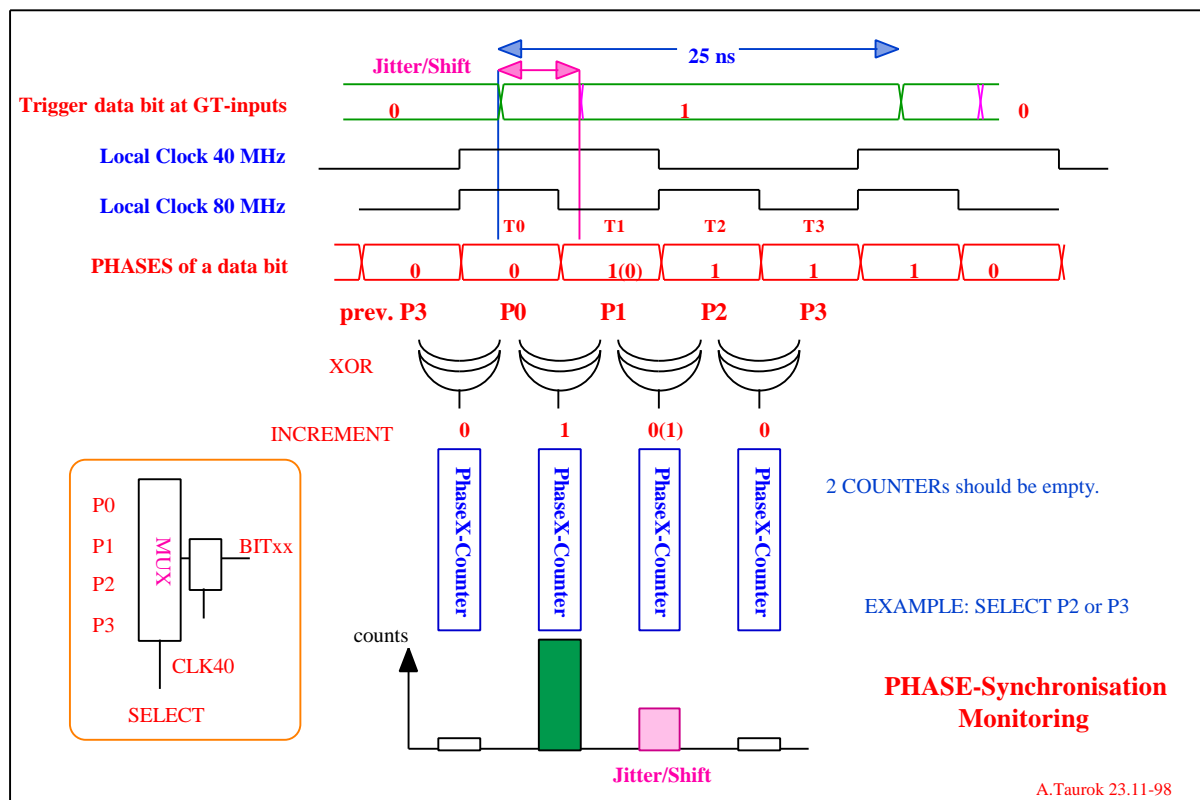


Fig.4 Monitoring

Conclusion:

A circuit has been designed to synchronise input data from different Level 1 Trigger sources to the local pipeline electronics. The phase synchronisation circuit is foreseen as the input stage for the bunch crossing synchronisation logic. General and specific timing constraints for the design in FPGA Xilinx chips have been given and adjustment and monitoring procedures were explained.

References:

- [1] The CMS Technical Proposal (sec. 9.4.5)
- [2] TTCrx Reference Manual, J. Christiansen, A. Marchioro and P. Moreira , July1997 Version 2.2
- [3] Trigger Review, Global Trigger Review, A. Taurok, 13 Nov 1998, CERN
<http://sungraz.cern.ch/CMS/trigger/globalTrigger/Welcome.html>
- [4] First Level Global Trigger for CMS A. Taurok, Second Workshop on Electronics for LHC Experiments, 23-27 Sept, Balatonfued CERN/LHCC/96-39