

PSB module **for the CMS Global Trigger Level 1**

Abstract:

The PSB (=Pipelined Synchronising Buffer) module synchronises all input channels to the same bunch crossing and sends them after a programmable delay to the logic modules.

The PSBs receive data from the Global Calorimeter Trigger and various so called 'technical' trigger signals. One set of synchronisation logic is foreseen for each pair of input channels. Error counters and DPMs (=dual port memories) exist for each individual channel.

FIFOs or PIPELINED REGISTERs are used to delay the input channels.

All features mentioned below might be changed slightly to improve the final module.

See drawing PSB_ovw.

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1. TRIGGER INPUT DATA ...options:

INPUT by CHANNEL LINK chipsProposal!!

We propose to use CHANNEL LINK chips to transfer data from the Global Calorimeter Trigger to the Global Trigger crate. A channel Link Transmitter chip accepts 21 bits at 40 MHz and sends them over 3 differential lines with a rate of 280 MHz to the Receiver. A fourth differential pair transfers the transmitter clock(40MHz). The receiver converts the data back to 21 bits at 40 MHz. The link can be used for distances up to 10 m (National Semiconductor DS90CR281/DS90CR282). On the PSB-Prototype module the input chips are placed on a small add-on board to allow different input options.

Parallel INPUT by LVDS signals or differential ECL or PECL

1. Problem: Not enough space on front panel for 12 input channels.
2. Problem: Large space for Receiver chips needed; complicated wiring.

INPUT Channels from the Global Calorimeter Trigger

See chapter: 'Interface Signals' on Global Trigger WEB-page.

2. FINE TIME ADJUSTMENT of INPUT CHANNELS

Monitoring and corrections:

(See Synchronisation Note CMS_IN99_010.pdf for more information.)

The parallel input data are sampled four times per bunch crossing and the best phase is selected to store the input data. The data transition time is checked continuously and errors are counted and the phases of one bit recorded.

No remarkable shifts in time should be caused by the clock distribution system. Only small time shifts are expected from output drivers due to variations in temperature and due to supply voltages.

3. BX-SYNCHRONISATION by FIFO memories (option 1):

See drawings *BX_sync1* and *PSB_xin1*.

Input data from the Global Calorimeter trigger arrive much earlier than Muons. Therefore they have to wait for nearly 20 bunch crossings.

1. WAIT for BX0 data.....synchronise all channels to the LHC-cycle

Starting with the local BC_Reset the logic waits a number of BXs, defined by the content of a WSTART register. *The WSTART value is equal to the (relative) latency time of the channel and should be adjusted to write data of BX=0 as the first word into the Synchronisation FIFO.* Close to or at the end of the LHC cycle the WSTOP register stops the input data so that the next BCRes synchronises again to the LHC cycle. The maximum difference between the local BX0 and the latest BX0-trigger word is limited by the length of the FIFO (64 words).

2. WAIT for latest channel.....synchronise channels to each other

As soon as the first word from the latest input channel has been stored, data from all channels are transferred to the following trigger logic modules (GTL). The RSTART register defines the common start point for the transfer. *The difference $RSTART-WSTART(i) = DELAY(i)$.*

Channel Link chips are used to transfer data via the backplane to the GTL module(s).

Remarks:

To assign trigger data correctly to their BX

- first the data arrival time at the trigger electronics and then

- all hardware delays of the clock distribution system, trigger logic and data links have to be known.

4. BX-SYNCHRONISATION by PIPELINE registers (option 2):

See drawing *PSB_syp1* and *BX_sync2*.

Input data are delayed using a pipeline register of a programmable length. The circuit is optimised for a very short delay (1bx). The minimum latency of the PSB module goes then down to 3 BX.: 1.FF=Receiver chip, 2.FF=SYNC-chip, 3.FF=Transmitter chip.

The synchronisation logic is similar as described above but without the WSTART register.

For a minimum latency time the local BCRes is sent >3 BX before the first BX from the LATEST channel arrives. The delay is then set to the minimum value of 1 BX and the RSTART register=1 to move the trigger data immediately to the GTL boards.

This circuit will be used too for Muon data on the Global Muon Trigger boards.

5. CHECKS FOR SYNCHRONISATION:

See drawing *BX_sync2*.

Check the GT electronics for BC counting errors:

The TIM module sends the BCReset every LHC cycle. With the new BCReset the contents of all local bunch counters are stored and checked for errors in the past LHC cycle. The 'LHCcycle'-monitoring data contain then this error information.

Resynchronisation:

Every LHC cycle a BcntReset is expected for resynchronisation. No data are lost due to the resynchronisation procedure. As the TTC system probably will not deliver the BCRreset continually a counter on the TIM board produces a BCRreset every LHC cycle to keep all Global Trigger modules synchronised to each other.

Bx synchronisation between crates: See drawing *BX_sync1*.

Without SYNC Flag: Compare data against constant SYNC-values or against the output of a counter (p.e: BX-number) during a selected gap. The software loads two registers (START_SY, STOP_SY) to define the synchronisation period. Only one sync period per LHC cycle is foreseen.

With SYNC Flag: Whenever a SYNC Flag arrives input data are checked against a constant value or against the current BX-number.

Check Transition time of input data:

Consecutive phase values are checked to each other to find the transition time of the input data. Differences are counted and read at the end of each LHC cycle. The distribution over the 4 counters show the stability of the data links.

6. PROCEDURE to synchronise MUON and CALORIMETER CHANNELS to each other:

See drawing *BX_sync2 and others...*

1. Adjust latest Muon channels to the LHC cycle:

(Pipeline delay circuit)

1.1 TTC sends BCRreset at a default time.

1.2 Set the DELAY to the minimum value

to get a minimum latency time in the Global Trigger.

Set RSTART to a default value.

DELAY changes the latency time.

RSTART starts to write data into DPM.

1.3 Check PLOTS from Global Monitoring data to find BX=0 in the data.

1.4 Set RSTART or maybe adjust BCRreset

to move data from BX=0 into DPM Address=0.

2. Find relative latency time of Calorimeter channels:

(FIFO delay circuit)

2.1 Set default values for the Calorimeter channels: WSTART=N=RSTART

WSTART defines BX0-data (=relative latency of CaloTrigger)

RSTART starts to write data into DPM

(DELAY= RSTART - WSTART)

2.2 Check PLOTS of trigger data to find BX=0.

2.3 Adjust WSTART=N'=RSTART (=min. delay)

to move data from BX=0 into DPM Address=0

2.4 The delay in the SYNC-FIFO is now defined by a later RSTART value.

3. Adjust all channels to each other by SYNC TRIGGERS

3.1 For each input channel set one trigger algorithm for SYNC data of the same BX.

3.2 Check then the algorithm bits in the FDL module (Global Monitoring data) to find the latency times for all channels.

3.3 Load the same RSTART value (=WSTART+delays) into all PSB modules and check again if SYNC data from all channels arrive at the same time in the Global Trigger Logic boards (GTL+FDL).

7. READOUT AFTER L1ACCEPT

GTFE interface:

A DPM dual port memory is used as a RING BUFFER. Every LHC cycle the BCRes signal resets the DPM address counters and therefore the address is equal to the bunch crossing number and data from the previous LHC cycle are overwritten.

The bunch crossing number of the L1Accept points then directly to the correct address in the Dual Port Memory. Data from several bunch crossings before and after the L1Accept are transferred to the Readout Processor, from where the data will be sent via the GTFE link to the GTFE(= Global Trigger Front End) module

Procedure:

A Readout Processor (ROP) receives an extraction request with the first bunch crossing number and an event number. The event number contains already a L1Acc/Mon flag. If a L1Accept has sent the extraction request the ROP sends the event number together with an Event-Identifier as the first word to the GTFE board. In case of a Global Monitoring request a Monitor-Identifier is sent. Then the ROP collects data from all Dual Port Memories (DPM). The procedure is repeated for a programmed number of bunch crossings. Finally an End_of_Event finishes the record.

On the GTFE board the first word is checked and data are moved either into the DAQ- or into the Monitor-memory.

A 32 bit word in the DPM contains 24 data bits, 3 parity bits, 1 sync flag and 4 phase bits
(=*Preliminary Format!!*)

Number of 32 bit words per event:

$5 \text{ BX} * 12 \text{ channels} + \text{eventnr} + \text{end_event} = 62 \text{ words/event}$

Time for data collection with 20 MHz: $t=50\text{ns} \times 62 = 3.1 * 10^{-6} \text{ sec} \ll 10 \mu\text{sec}$ for 100 kHz trigger rate. Therefore nearly 70% of time is available for Global Monitoring requests.

8. GLOBAL MONITORING

The time between L1Accepts is used to read data from the DPM memories containing a precise copy of the output data stream. As described above the Monitoring task uses the same electronics on the PSB and GTF as the normal Event Readout task. On the GTFE board the monitoring data are written into different DPM chips. Compared to the maximum trigger rate theoretically 2 times more monitoring information can be extracted from DPMs on the PSB and GTF boards.

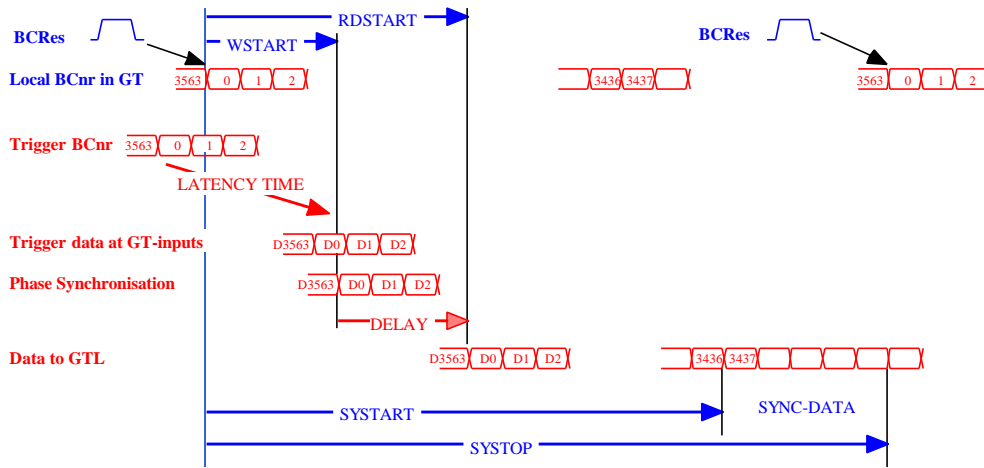
9. ERROR CHECKS with every LHC cycle

At the end of every LHC cycle the content of several counters is saved.

The Phase-, Status- and Error registers are read by a VME based monitoring program. Even fatal errors do not stop the electronics. The monitoring program has to run synchronously to the LHC cycle.

Check for synchronisation errors during data taking:

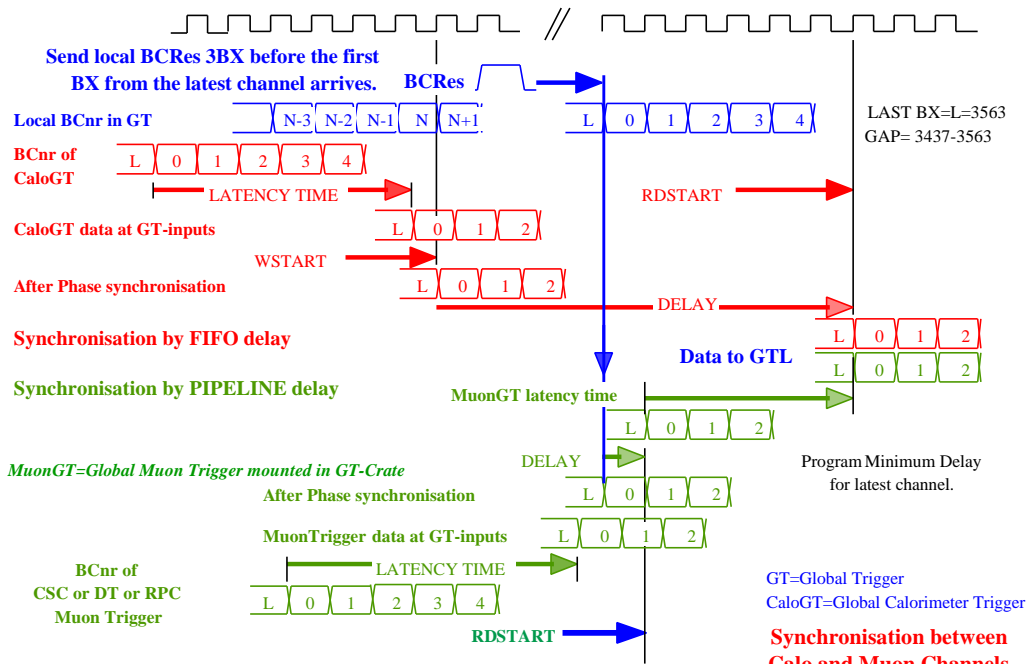
After the adjustment no synchronisation and parity errors should appear if the upstream trigger logic and the PSB channel use the same synchronisation and parity mode. A small logic checks the synchronisation words against a constant value or against a local counter and increments a counter in case of an error. At the end of a LHC cycle the content of the error counter is saved and is available for VME access during the following LHC cycle. This logic guarantees a continuous check for every LHC cycle and does not interfere with the run.



LAST BX=L=3563
GAP= 3437-3563

BX-Synchronisation PSB

A.Taurok 27.10-98 BX_SYNC1.cdd



Synchronisation between Calo and Muon Channels PSB

A.Taurok 5.11-98 BX_SYNC2.cdd

