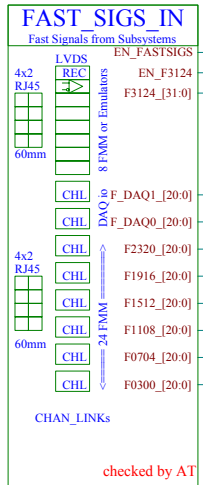
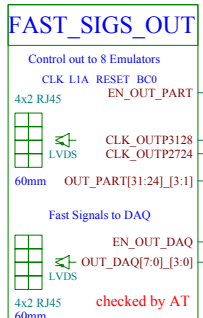
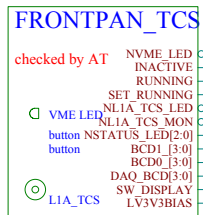


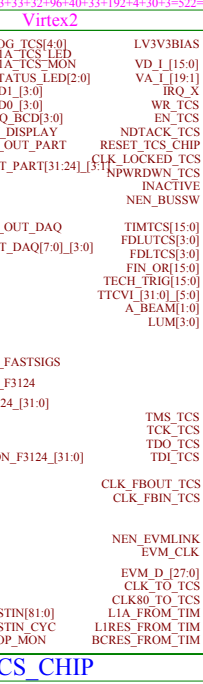
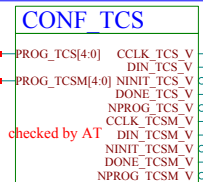
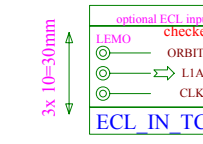
Accepted by Greg Iles 27.8.02:

Encoded Signals to EMULATORS:
 (BC0,RESET,LIA)= (0,0,0) => 'inactive'
 (BC0,RESET,LIA)= (0,0,1) => LIA
 (BC0,RESET,LIA)= (0,1,0) => RESYNC(LIReset)
 (BC0,RESET,LIA)= (0,1,1) => Reset Event Counter
 (BC0,RESET,LIA)= (1,0,0) => BC0
 (BC0,RESET,LIA)= (1,0,1) => Reset OrbitCounter
 (BC0,RESET,LIA)= (others) => forbidden

BIT Assignments:
 3 = BC0
 2 = RESET
 1 = LIA
 0 = CLK_P



converted Fast Signals
 1 Chan.Link could carry the 5th channel of the CONV6U receiver board.

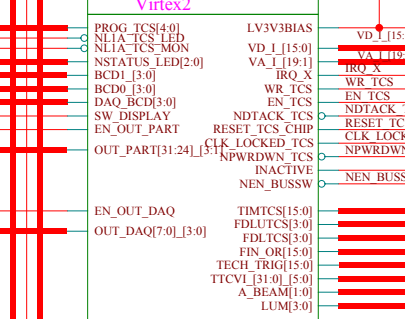


immediate Fast Signals

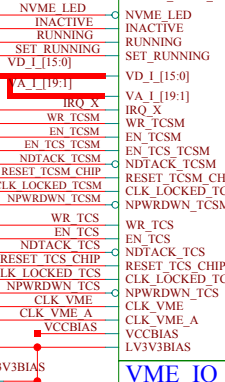
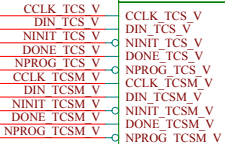
LUM[*] are normal signals

TCS MON CHIP

20 (R-term) +2(clk) =22 pins
 2+12+12+33+33+32+96+40+33+192+4+30+3+52=XC2V2000

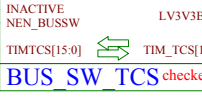


TCS_CHIP



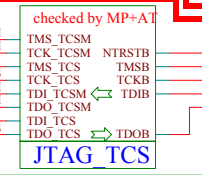
checked by HB+AT

VME IO_TCS



checked by AT

BUS_SW_TCS



checked by MP+AT

JTAG_TCS

ChanLinks to GTFE



checked by MP+AT

RO TCS

checked by AT

RO-bus

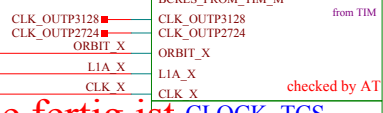


ZPACK_TCS

TCS-BOARD-9U

TCS9U

HEPHY VIENNA ELEKTRONIK I	sheet 1 of 2
modified by: M.PADRTA	10-30-2003_11:16
checked by: AT+MP	30.10.2003

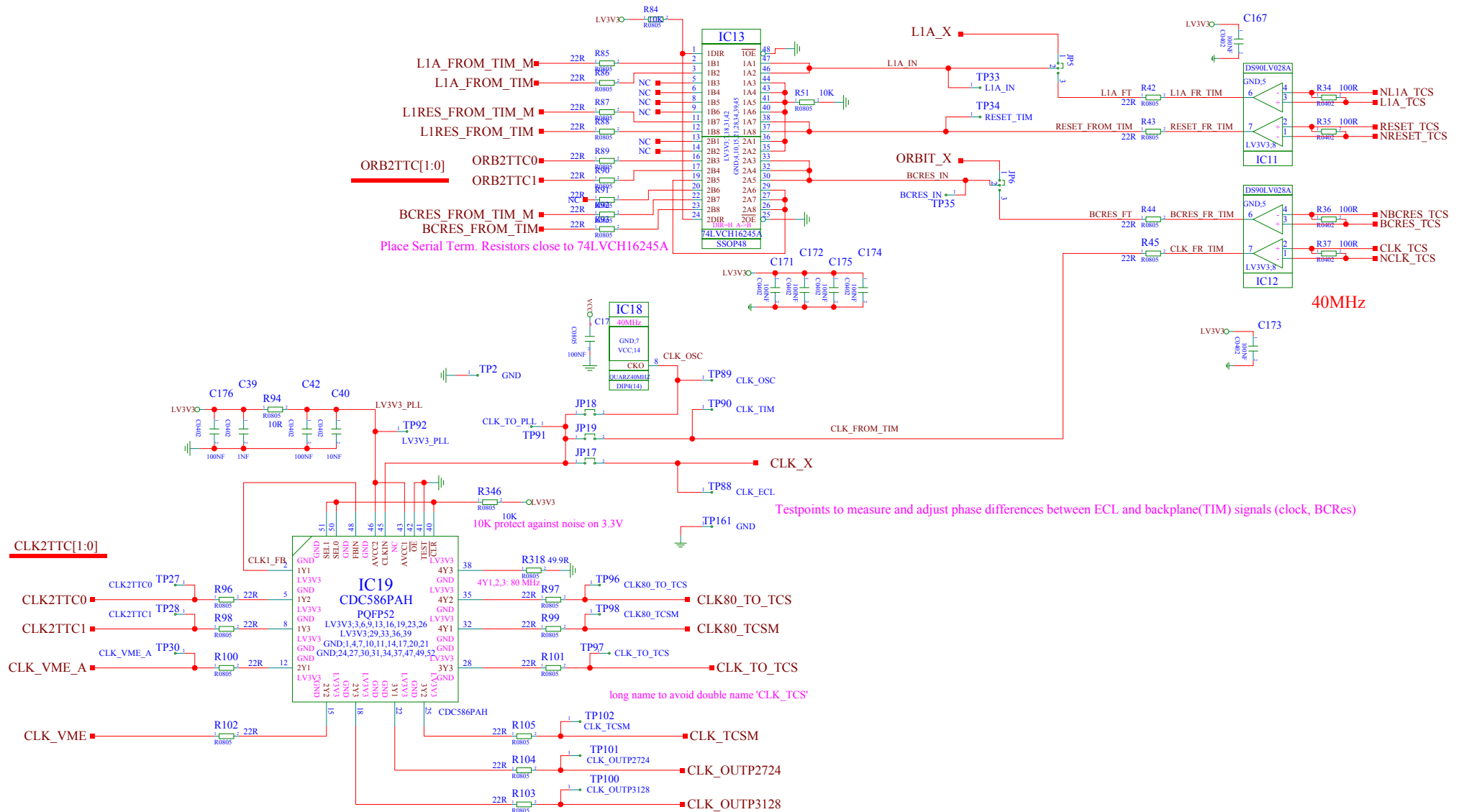


checked by AT
 +1.5V/2A
 +1.8V/70mA
 POWER_TCS

Alle Schaltpläne als Abschluß "lesbar" machen, wenn Platine fertig ist

Optionally the ECL signals LIA_X and CLK_X might be used
Frontpanel ECL signals

LVDS signals from TIM card via Backplane



Place Test points for internal CLOCK signals close to receiving chips.

Place Serial Term. Resistors close to CDC586

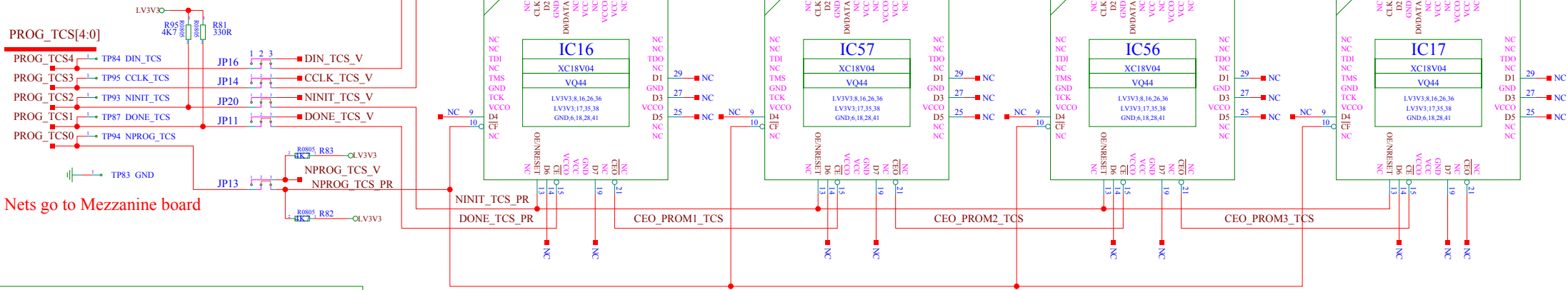


<h1>TCS-CARD-9U</h1>	
<h2>CLOCK TCS</h2>	
HEPHY VIENNA ELEKTRONIK I	sheet 1 of 1
modified by: M.PADRTA	10-28-2003_11:05
checked by: A.TAUROK	24.10.03

TCS chip

4 Proms to load also a Virtex4000 chip

SWITCH BETWEEN PROM - OR VME- PROGRAMMING



Nets go to Mezzanine board

On page 2 of TCS_CHIP you find:
 HSWAP_EN_TCS
 NPWRDWN_B
 DOUT_TCS
 On Mezzanine board for TCS you find: M0,M1,M2

1st PROM

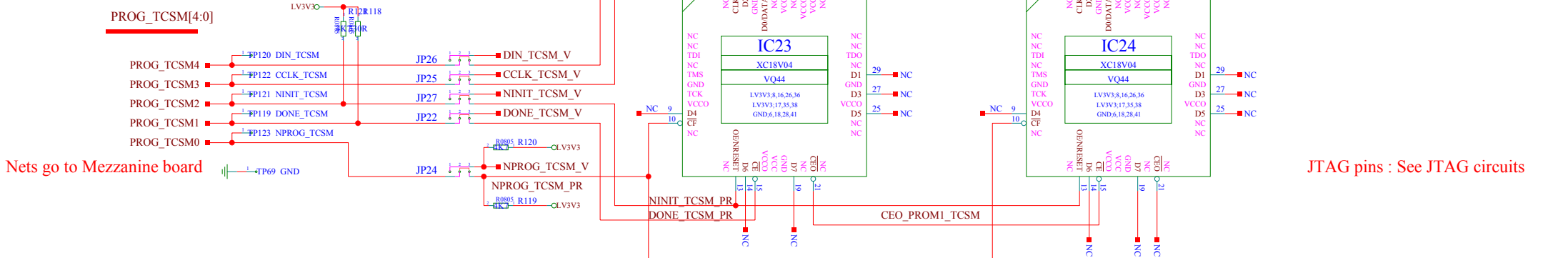
2nd PROM

3rd PROM

4th PROM

TCSM chip

SWITCH BETWEEN PROM - OR VME- PROGRAMMING



Nets go to Mezzanine board

See MasterSerialMode in XC18V00 Datasheet Fig. 6 on Pg. 10
 On page 2 of TCSM_CHIP you find:
 HSWAP_EN_TCSM
 NPWRDWN_B
 DOUT_TCSM
 On Mezzanine board for TCSM you find: M0,M1,M2

If PROM are used for configuration then set TCS, TCSMON chip in MasterSerialMode (M0=M1=M2=0)

Selecting Configuration Modes

The XC18V00 accommodates serial and parallel methods of configuration. The configuration modes are selectable through a user control register in the XC18V00 device. This control register is accessible through JTAG, and is set using the "Parallel mode" setting on the Xilinx JTAG Programmer software. Serial output is the default programming mode.

cascaded PROM

JTAG pins : See JTAG circuits

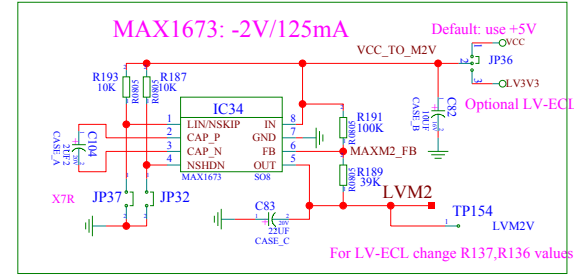
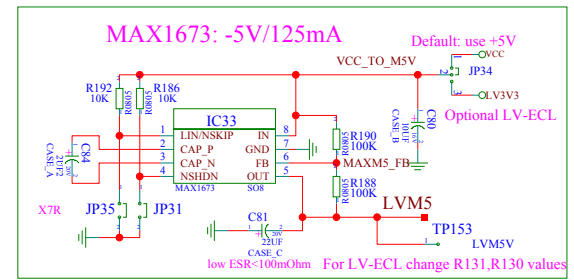
TCS-CARD-9U	
CONF TCS	
HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 1
modified by: A.T	10-23-2003_17:20
checked by: A.TAUROK	23.10.03

LEMO for front panel

INPUT Signals

PECL+3.3V,10k: $V_{ih}=2.2\dots2.5$ $V_{il}=1.4\dots1.75$, $V_{BB}=2.0$
 PECL+5V,10k: $V_{ih}=3.9..4.0..4.2$, $V_{il}=3.0..3.3\dots3.5$, $V_{BB}=+3.7$
 ECL-5V,10k: $V_{ih}=-1.1\dots-1.0\dots-0.8$, $V_{il}=-1.9\dots-1.7\dots-1.5$, $V_{BB}=-1.3$
 PECL(+5V) to LVTTTL: LVELT23, EPT23, EPT21
 LVPECL(+3.3V) to LVTTTL: LVELT23, EPT23, EPT21,EPT26
 ECL (-5.2V) to TTL: MC10H125(4x), H601(9x), ELT25
 ECL(-5.2V) to LVTTTL: EPT25(diff)
 LVECL (-3.3V) to TTL: ELT25, //to LVTTTL: EPT25(diff)

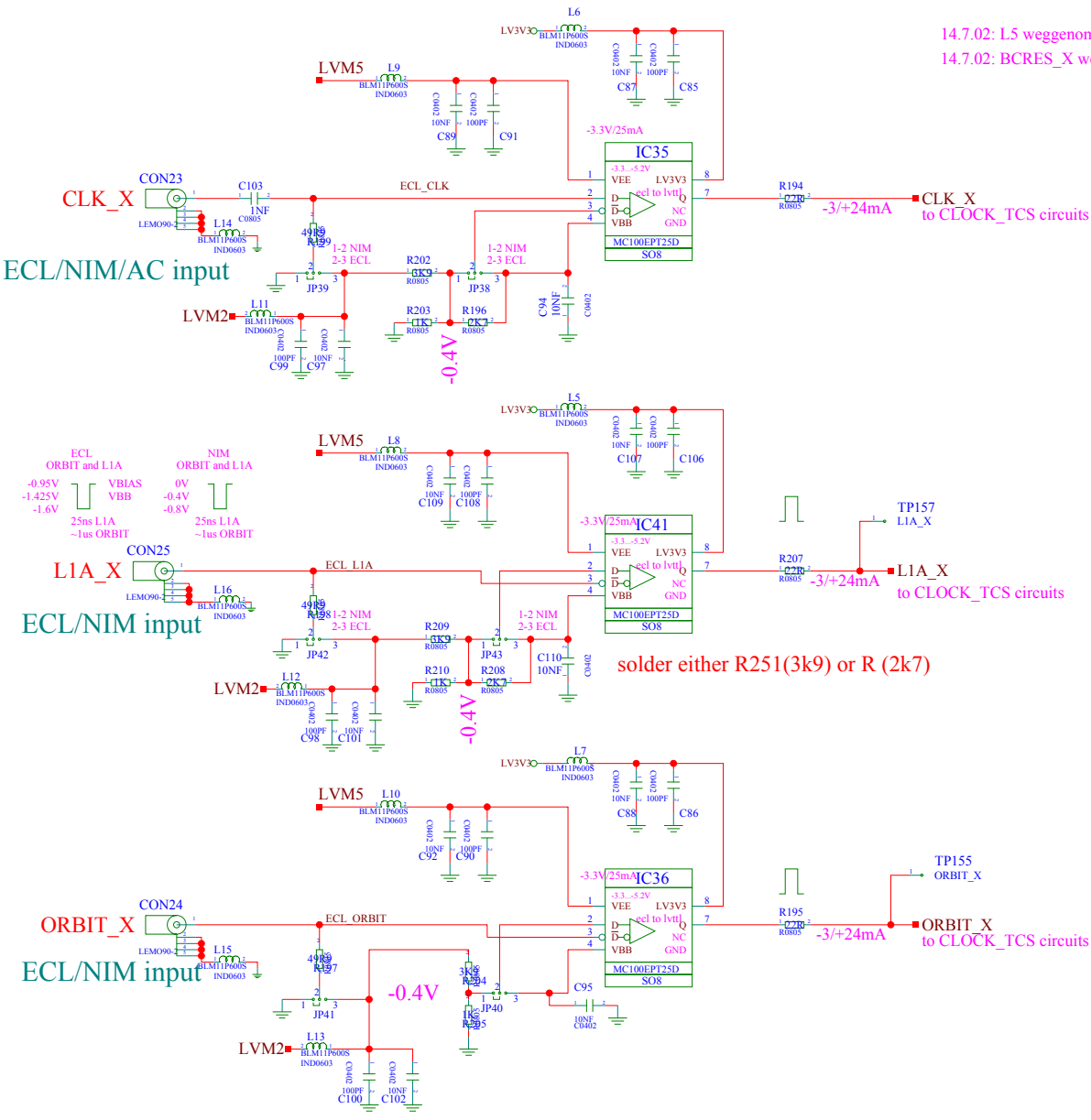
default:
JP18, JP19
JP17, JP20



Ripple noise 150mV with: 2.2 and 22 uF
 Ripple noise 50mV with: 4.7 and 47 uF
 Max. I_term: (2-8V)/50=24mA => 72mA for LVM2
 Max. IEE/chip= 25mA=> 75 mA for LVM5

ECL (-5.2V) to TTL: 4 gates, MC10H125FN plcc20, 46 Stk a \$3.24
 ON-Semiconductor onsemi.com
 MC100EPT21D: diff LVPECL to LVTTTL, SOIC8 98Stk a \$5.8
 MC100EPT23: 3.3V 2x diff PECL to 24mA LVTTTL, SOIC8 98Stk a \$5.8
 MC100EPT25: diff ECL/LVECL to LVTTTL
 MC100LVELT23D 2x diff 3.3VPECL to LVTTTL24mA, SOIC8 98Stk a \$4.44
 MICREL.com
 SY10ELT21: diff PECL to TTL (Micrel)
 SY10ELT21L: diff 3.3V PECL to TTL (Micrel)

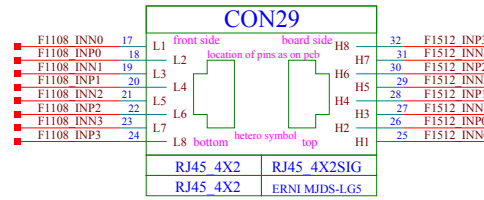
<h1>TCS-CARD</h1>	
<h2>ECL IN TCS</h2>	
HEPHY VIENNA ELEKTRONIK I	sheet 1 of 1
modified by: M:PADRTA	10-17-2003_18:07
checked by: A.TAUROK	17.10.03



14.7.02: L5 weggenommen
 14.7.02: BCRES_X weggenommen

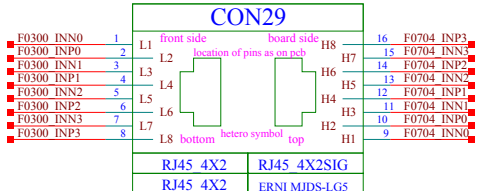
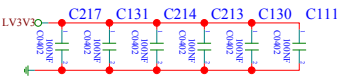
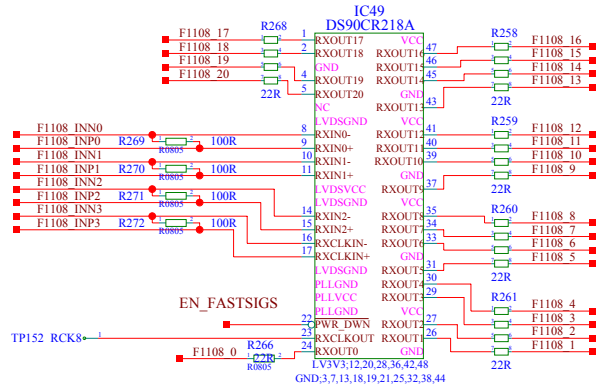
solder either R251(3k9) or R (2k7)

Mounted on TOP side



Partitions 11, 10, 9, 8

Partitions 15, 14, 13, 12

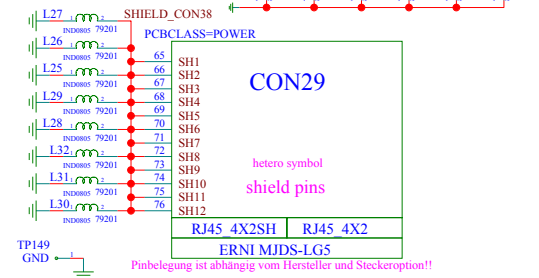
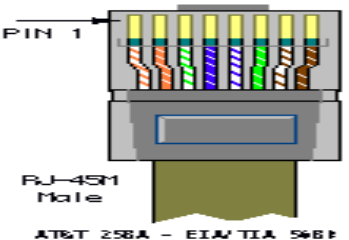
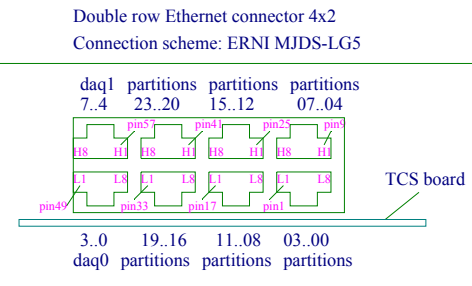
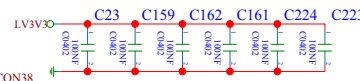
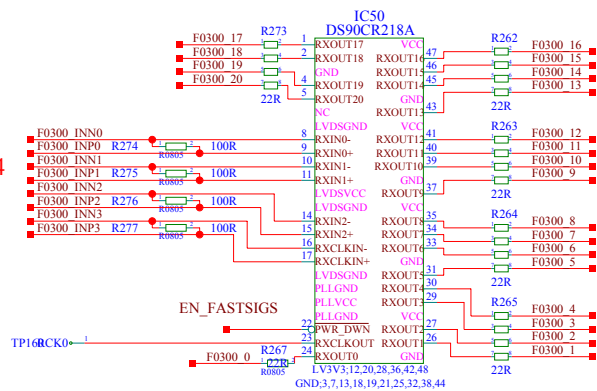


Partitions 3, 2, 1, 0

Partitions 7, 6, 5, 4

PIN Layout on RJ45 for Channel Links.
agrees with CONV6U boards

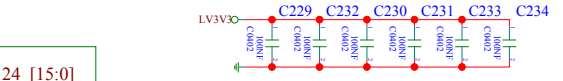
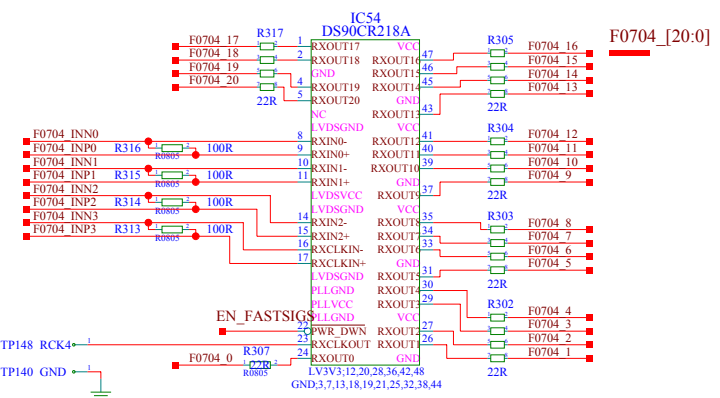
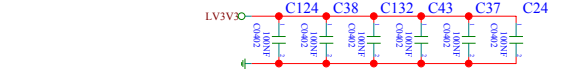
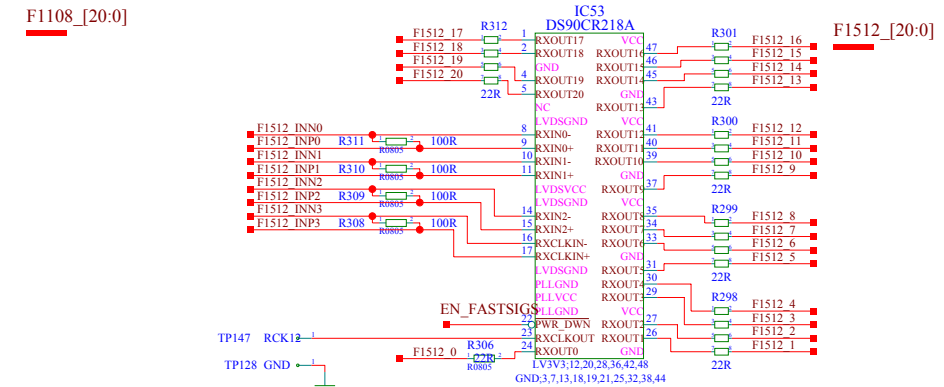
Same PIN Layout on RJ45 as for PSBIN prototype.



CHLINK connectors used as receivers SHIELD pins

Example: F1108_.....=> bits for Partitions 11, 10, 9, 8

Mounted on BOTTOM side



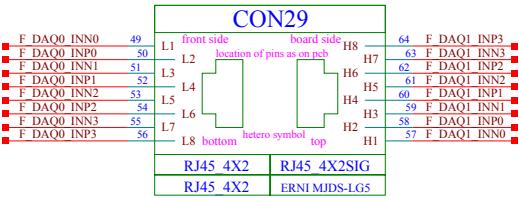
- 8 Emulators or partitions — F3124_[15:0]
- 24 partitions — F2320_[20:0]
- F1916_[20:0]
- F1512_[20:0]
- F0704_[20:0]
- F0300_[20:0]
- 8 DAQ partitions — F_DAQ1_[20:0]
- F_DAQ0_[20:0]

FAST SIGNALS
from partitions 0.....15

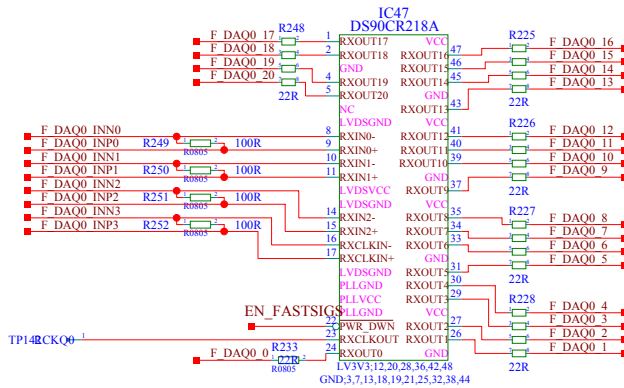
TCS-BOARD-9U
FAST SIGS IN

HEPHY VIENNA ELEKTRONIK I	sheet 1 of 3
modified by: M:PADRTA	10-28-2003_10:45
checked by: A.TAUROK	23.10.03

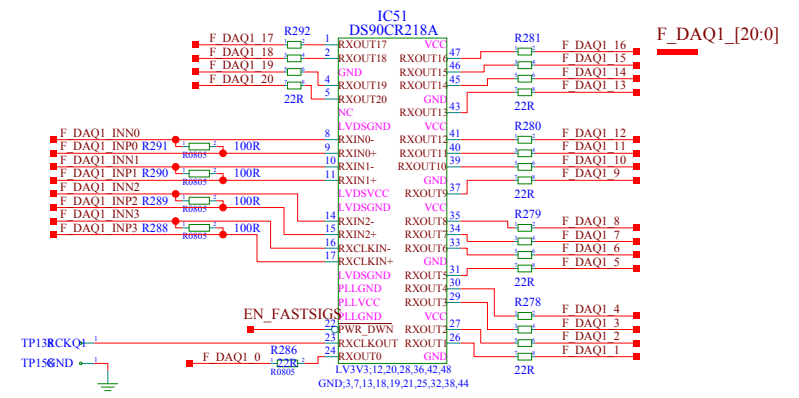
FAST SIGNALS from DAQ partitions



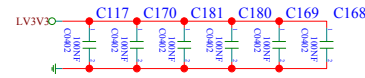
DAQ Partitions 3,2,1,0 DAQ Partitions 7,6,5,4



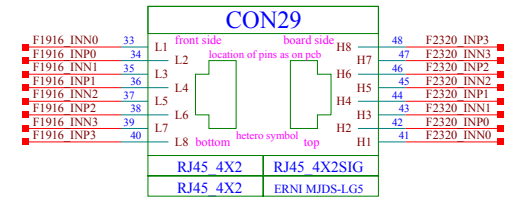
F_DAQ0_[20:0]



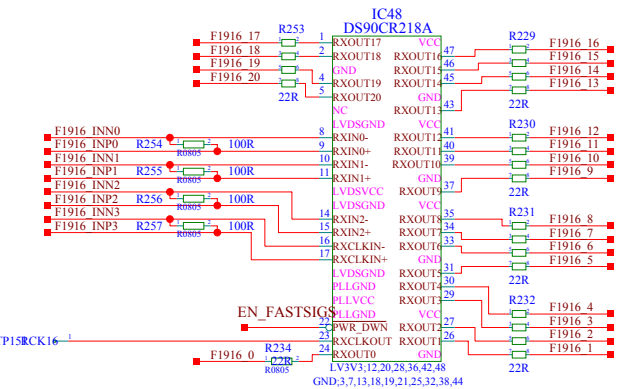
F_DAQ1_[20:0]



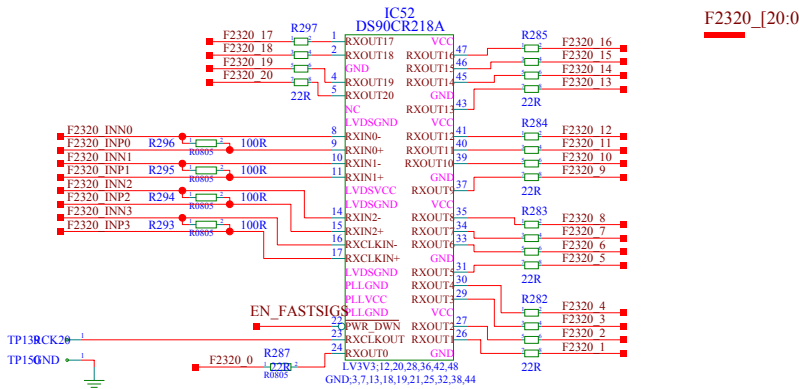
Board Edge



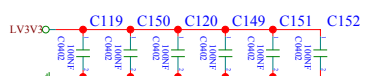
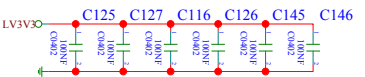
Partitions 19, 18, 17, 16 Partitions 23, 22, 21, 20



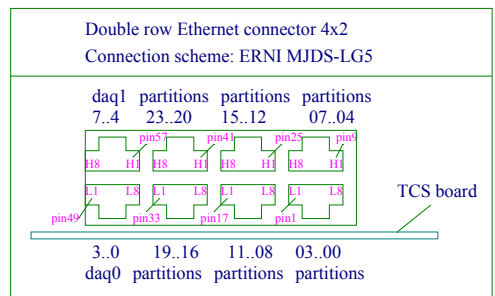
F1916_[20:0]



F2320_[20:0]



PIN Layout on RJ45 for Channel Links.



FAST SIGNALS from partitions 16...23

TCS-BOARD-9U	
FAST SIGS IN	
HEPHY VIENNA ELEKTRONIK I	sheet 2 of 3
modified by: M:PADRTA	10-28-2003_10:45
checked by: A.TAUROK	23.10.03

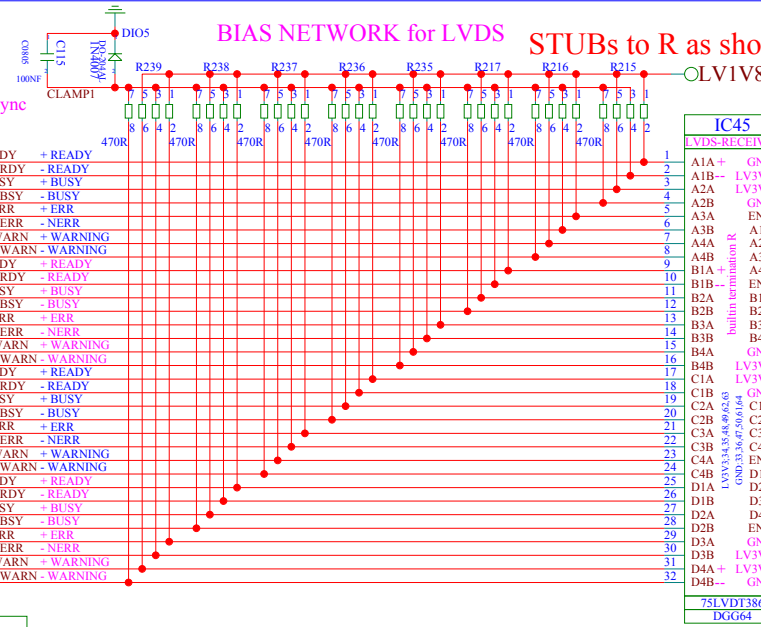
Hot Swap schematic in TCS-Chip schematics

BIT Assignments:

- bit 3 = READY
- bit 2 = BUSY
- bit 1 = ERR/Out_of_Sync
- bit 0 = WARNING

BIAS NETWORK for LVDS

STUBS to R as short as possible

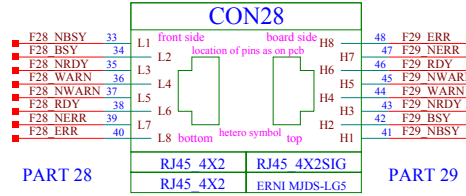
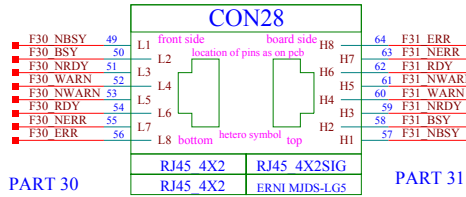


IC45		LVDS-RECEIVER	
A1A+	GND	60	
A1B-	LV3V3	59	
A2A	LV3V3	58	
A2B	GND	57	
A3A	ENA	56	
A3B	A1Y	55	
A4A	A2Y	54	
A4B	A3Y	53	
A4Y	A4Y	52	
B1A	ENB	51	
B1B	B1Y	50	
B2A	B2Y	49	
B2B	B3Y	48	
B3A	B3Y	47	
B3B	B4Y	46	
B4A	GND	45	
B4B	LV3V3	44	
C1A	LV3V3	43	
C1B	GND	42	
C2A	C1Y	41	
C2B	C2Y	40	
C3A	C3Y	39	
C3B	C4Y	38	
C4A	ENY	37	
C4B	D1Y	36	
D1A	D2Y	35	
D1B	D3Y	34	
D2A	D4Y	33	
D2B	END	32	
D3A	GND	31	
D3B	LV3V3	30	
D4A	LV3V3	29	
D4B	GND	28	
75LVD1386			
DGG64			

BIT Assignments:

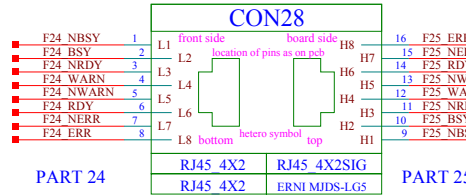
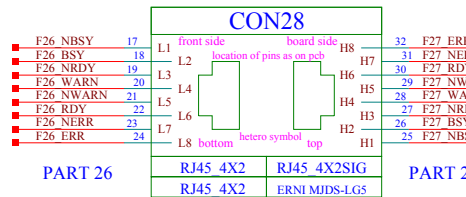
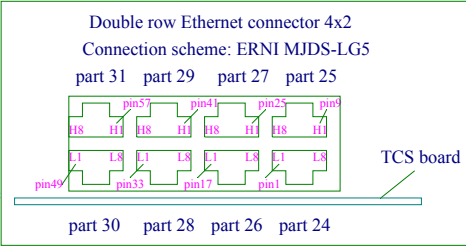
- bit 3 = READY
- bit 2 = BUSY
- bit 1 = Out_of_Sync / ERR
- bit 0 = WARNING

F3124_[31:0]



FAST SIGNAL PINS

- PIN1 - BUSY
- PIN2 + BUSY
- PIN3 - READY
- PIN4 + WARNING
- PIN5 - WARNING
- PIN6 + READY
- PIN7 - ERR/out of sync
- PIN8 + ERR/out of sync



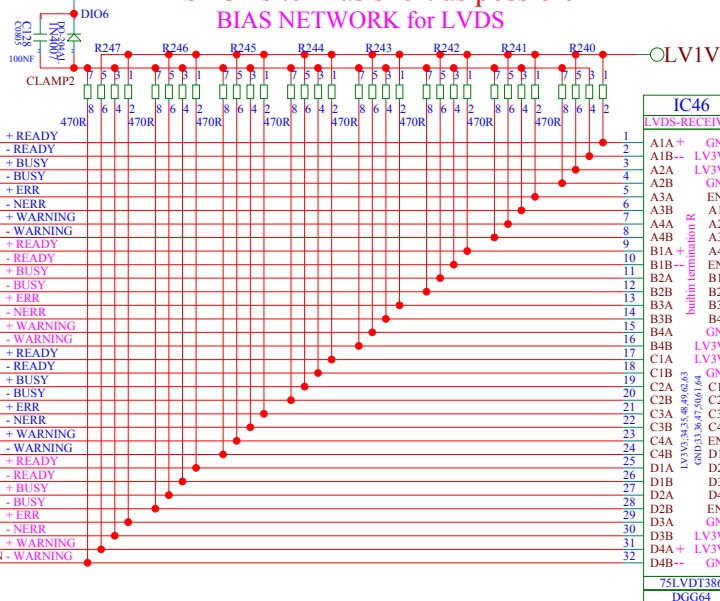
PIN Layout on RJ45 for FMM signals

CONNECTION of PINS according to FMM definition
FMM = Fast Monitoring Module for partitions

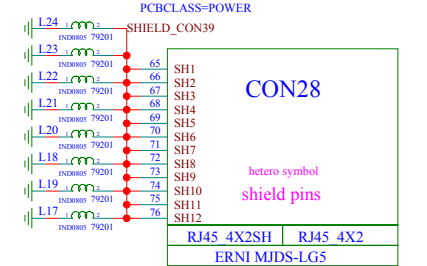
LVDS387 drives 350mV -10dB of 20m cable (350mV+0.3162)=110 mV > 100 mV of LVDS386
Driver common mode voltages: LVDS387 = +1.3V; DS90LV047A...+1.2V
LVDS386 rec. accepts common mode voltage = +0.3...+2.3 V

STUBS to R as short as possible

BIAS NETWORK for LVDS



IC46		LVDS-RECEIVER	
A1A+	GND	60	
A1B-	LV3V3	59	
A2A	LV3V3	58	
A2B	GND	57	
A3A	ENA	56	
A3B	A1Y	55	
A4A	A2Y	54	
A4B	A3Y	53	
A4Y	A4Y	52	
B1A	ENB	51	
B1B	B1Y	50	
B2A	B2Y	49	
B2B	B3Y	48	
B3A	B3Y	47	
B3B	B4Y	46	
B4A	GND	45	
B4B	LV3V3	44	
C1A	LV3V3	43	
C1B	GND	42	
C2A	C1Y	41	
C2B	C2Y	40	
C3A	C3Y	39	
C3B	C4Y	38	
C4A	ENC	37	
C4B	D1Y	36	
D1A	D2Y	35	
D1B	D3Y	34	
D2A	D4Y	33	
D2B	END	32	
D3A	GND	31	
D3B	LV3V3	30	
D4A	LV3V3	29	
D4B	GND	28	
75LVD1386			
DGG64			



SHIELD PINS

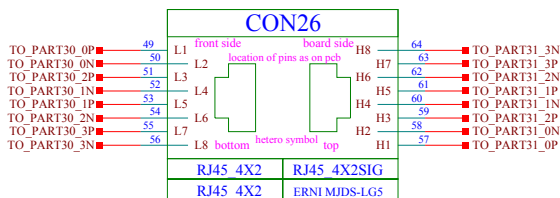
Not converted
FAST SIGNALS from EMULATORS
or directly from FMMs

TCS-BOARD-9U
FAST SIGS IN

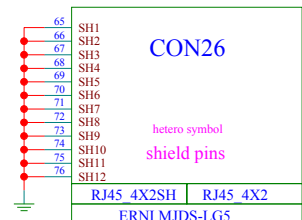
BIT Assignment:

- 3 = BC0
- 2 = RESET
- 1 = LIA
- 0 = CLK_P

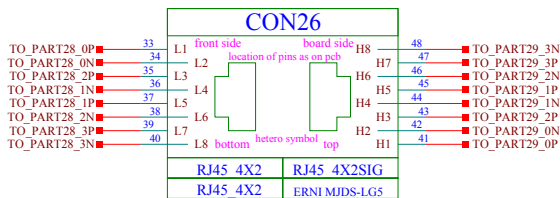
- 1 = CLK_P (bit0)
- 2 = CLK_N (bit0)
- 3 = RESET_P (bit2)
- 4 = LIA_N (bit1)
- 5 = LIA_P (bit1)
- 6 = RESET_N (bit2)
- 7 = BC0_P (bit3)
- 8 = BC0_N (bit3)



- 8 = BC0_N (bit3)
- 7 = BC0_P (bit3)
- 6 = RESET_N (bit2)
- 5 = LIA_P (bit1)
- 4 = LIA_N (bit1)
- 3 = RESET_P (bit2)
- 2 = CLK_N (bit0)
- 1 = CLK_P (bit0)

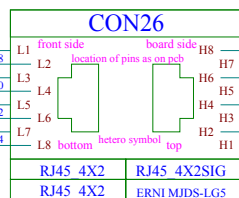


Pinbelegung ist abhängig vom Hersteller und Steckertyp!!!
Output connector ==> Shield connected to GND



BIASING RESISTOR NETWORK??

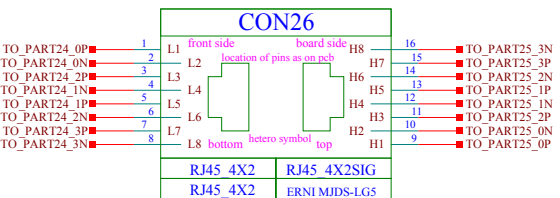
- 1 = CLK_P (bit0)
- 2 = CLK_N (bit0)
- 3 = RESET_P (bit2)
- 4 = LIA_N (bit1)
- 5 = LIA_P (bit1)
- 6 = RESET_N (bit2)
- 7 = BC0_P (bit3)
- 8 = BC0_N (bit3)



- 8 = BC0_N (bit3)
- 7 = BC0_P (bit3)
- 6 = RESET_N (bit2)
- 5 = LIA_P (bit1)
- 4 = LIA_N (bit1)
- 3 = RESET_P (bit2)
- 2 = CLK_N (bit0)
- 1 = CLK_P (bit0)

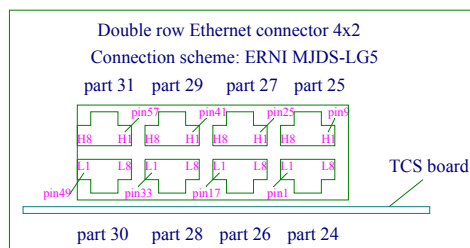
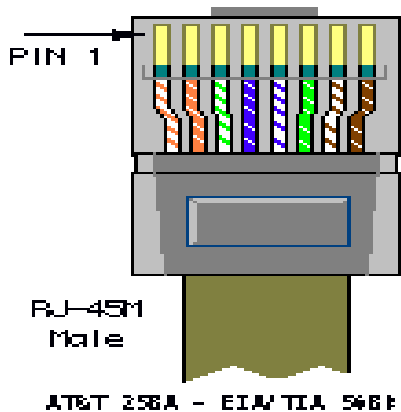
APVE definition

- 1 = CLK_P
- 2 = CLK_N
- 3 = RESET_P
- 4 = LIA_N
- 5 = LIA_P
- 6 = RESET_N
- 7 = BC0_P
- 8 = BC0_N

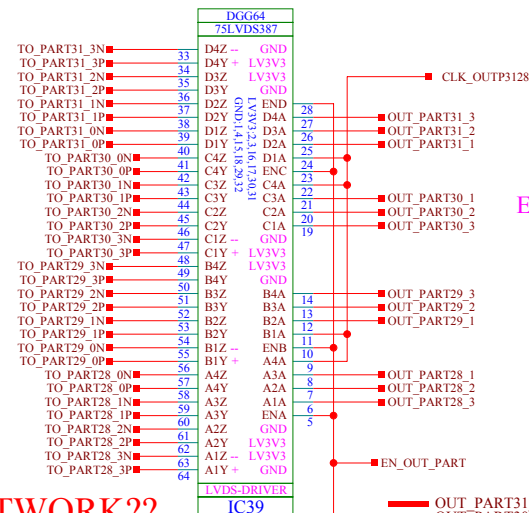


PIN LAYOUT for EMULATORS.

Pin-layout agreed with APVE

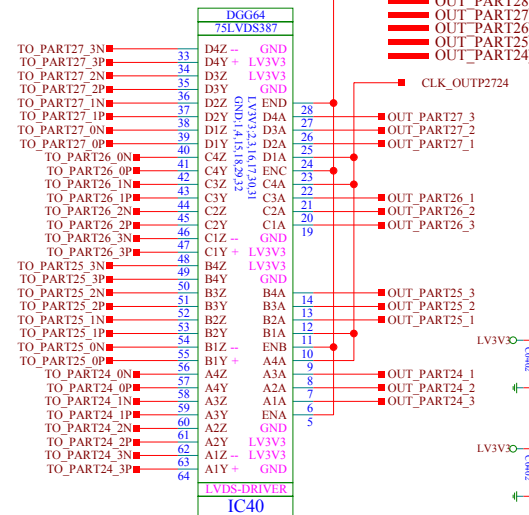


Hyperlynx Simulation with Zdiff=100 cable up to 20 m has been done. using Zo=83 conn instead of Ethernet conn.

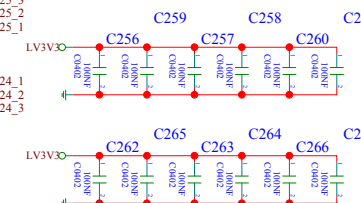


Encoded Signals:

- (BC0,RESET,LIA)=(0,0,0) => 'inactive'
- (BC0,RESET,LIA)=(0,0,1) => LIA
- (BC0,RESET,LIA)=(0,1,0) => RESYNC(L)
- (BC0,RESET,LIA)=(0,1,1) => Reset Event
- (BC0,RESET,LIA)=(1,0,0) => BC0
- (BC0,RESET,LIA)=(1,0,1) => Reset Orbit
- (BC0,RESET,LIA)=(others) => forbidden



OUT_PART[31:24]_[3:1] (bus name of Symbol)



Pin assignm. on LVDS387 optimized for diff.signals.
Attention: Chips are turned over for better routing to Front Side
LVDS387: Y=pos. Z=neg.output

Output to 8 Emulator

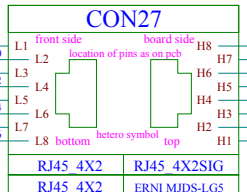
TCS-BOARD-9U		
FAST SIGS OUT		
HEPHY VIENNA ELEKTRONIK I	sheet 1 of 2	
modified by: M.PADRTA	10-28-2003_10:51	
checked by: A.TAUROK	17.10.2003	

FAST SIGNAL PINS

- PIN1 - BUSY (bit2)
- PIN2 + BUSY (bit2)
- PIN3 - READY (bit3)
- PIN4 + WARNING (bit0)
- PIN5 - WARNING (bit0)
- PIN6 + READY (bit3)
- PIN7 - ERR (bit1)
- PIN8 + ERR (bit1)

DAQ6

- TO_DAQ6_2N 49
- TO_DAQ6_2P 50
- TO_DAQ6_3N 51
- TO_DAQ6_3P 52
- TO_DAQ6_0N 53
- TO_DAQ6_0P 54
- TO_DAQ6_1N 55
- TO_DAQ6_1P 56



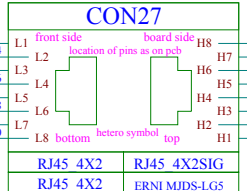
DAQ7

- TO_DAQ7_1P 64
- TO_DAQ7_1N 63
- TO_DAQ7_3P 62
- TO_DAQ7_3N 61
- TO_DAQ7_0N 60
- TO_DAQ7_0P 59
- TO_DAQ7_2P 58
- TO_DAQ7_2N 57

- PIN8 + ERR (bit1)
- PIN7 - ERR (bit1)
- PIN6 + READY (bit3)
- PIN5 - WARNING (bit0)
- PIN4 + WARNING (bit0)
- PIN3 - READY (bit3)
- PIN2 + BUSY (bit2)
- PIN1 - BUSY (bit2)

DAQ4

- TO_DAQ4_2N 33
- TO_DAQ4_2P 34
- TO_DAQ4_3N 35
- TO_DAQ4_3P 36
- TO_DAQ4_0N 37
- TO_DAQ4_0P 38
- TO_DAQ4_1N 39
- TO_DAQ4_1P 40



DAQ5

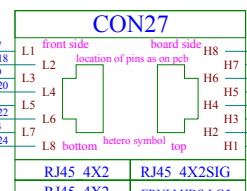
- TO_DAQ5_1P 48
- TO_DAQ5_1N 47
- TO_DAQ5_3P 46
- TO_DAQ5_3N 45
- TO_DAQ5_0N 44
- TO_DAQ5_0P 43
- TO_DAQ5_2P 42
- TO_DAQ5_2N 41

- PIN8 + ERR (bit1)
- PIN7 - ERR (bit1)
- PIN6 + READY (bit3)
- PIN5 - WARNING (bit0)
- PIN4 + WARNING (bit0)
- PIN3 - READY (bit3)
- PIN2 + BUSY (bit2)
- PIN1 - BUSY (bit2)

PIN Layout on RJ45 according to FMM definition.
See CMS Note 2002/033 CMS L1 Trigger Control System

DAQ2

- TO_DAQ2_2N 17
- TO_DAQ2_2P 18
- TO_DAQ2_3N 19
- TO_DAQ2_3P 20
- TO_DAQ2_0N 21
- TO_DAQ2_0P 22
- TO_DAQ2_1N 23
- TO_DAQ2_1P 24



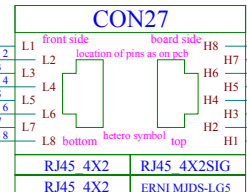
DAQ3

- TO_DAQ3_1P 32
- TO_DAQ3_1N 31
- TO_DAQ3_3P 30
- TO_DAQ3_3N 29
- TO_DAQ3_0N 28
- TO_DAQ3_0P 27
- TO_DAQ3_2P 26
- TO_DAQ3_2N 25

- PIN8 + ERR (bit1)
- PIN7 - ERR (bit1)
- PIN6 + READY (bit3)
- PIN5 - WARNING (bit0)
- PIN4 + WARNING (bit0)
- PIN3 - READY (bit3)
- PIN2 + BUSY (bit2)
- PIN1 - BUSY (bit2)

DAQ0

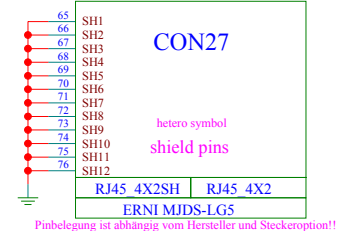
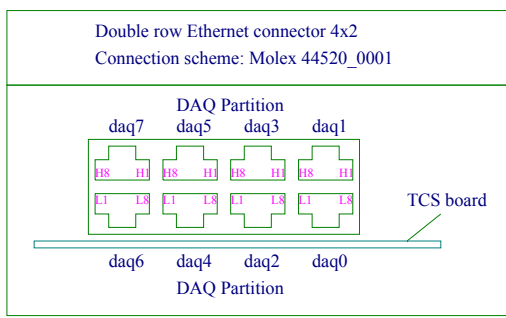
- TO_DAQ0_2N 1
- TO_DAQ0_2P 2
- TO_DAQ0_3N 3
- TO_DAQ0_3P 4
- TO_DAQ0_0N 5
- TO_DAQ0_0P 6
- TO_DAQ0_1N 7
- TO_DAQ0_1P 8



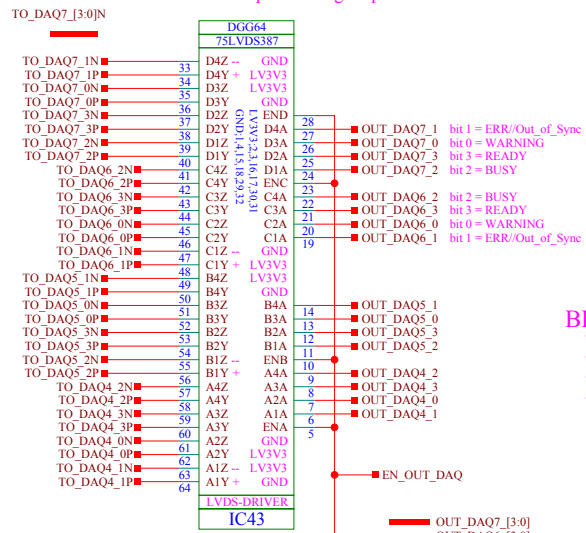
DAQ1

- TO_DAQ1_1P 16
- TO_DAQ1_1N 15
- TO_DAQ1_3P 14
- TO_DAQ1_3N 13
- TO_DAQ1_0N 12
- TO_DAQ1_0P 11
- TO_DAQ1_2P 10
- TO_DAQ1_2N 9

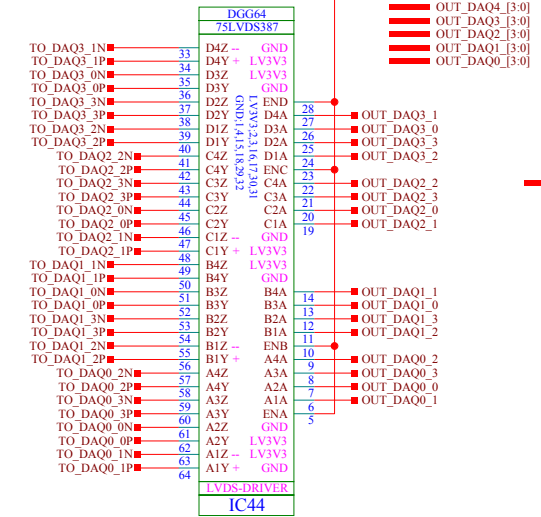
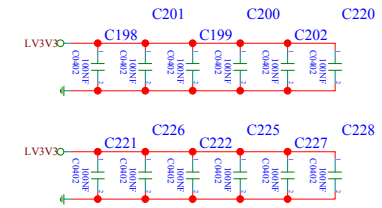
- PIN8 + ERR (bit1)
- PIN7 - ERR (bit1)
- PIN6 + READY (bit3)
- PIN5 - WARNING (bit0)
- PIN4 + WARNING (bit0)
- PIN3 - READY (bit3)
- PIN2 + BUSY (bit2)
- PIN1 - BUSY (bit2)



LVDS387: Y=pos. Z=neg.output



BIT Assignments:
bit 3 = READY
bit 2 = BUSY
bit 1 = ERR/Out_of_Sync
bit 0 = WARNING



OUT_DAQ[7:0]_[3:0]

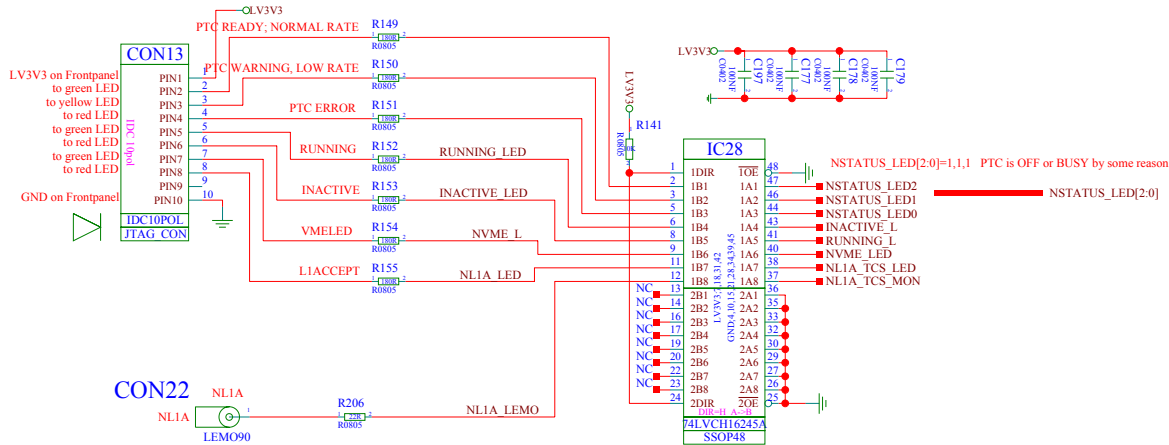
OUTPUT to 8 DAQ partitions.

TCS-BOARD-9U
FAST SIGS OUT

HEPHY VIENNA ELEKTRONIK I	sheet 2 of 2
modified by: M.PADRTA	10-17-2003_17:23
checked by: A.TAUROK	17.10.2003

DISPLAY mounted above all connectors

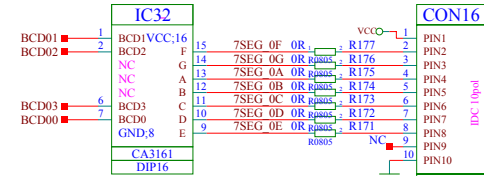
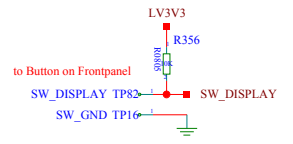
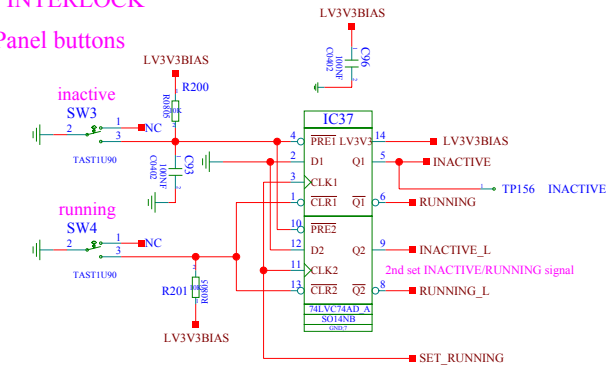
Inverted signals drive LEDs.



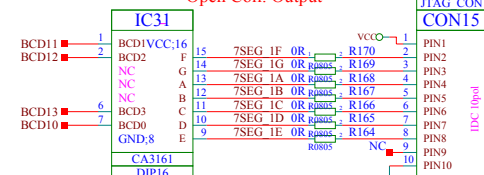
INTERLOCK

Front Panel buttons

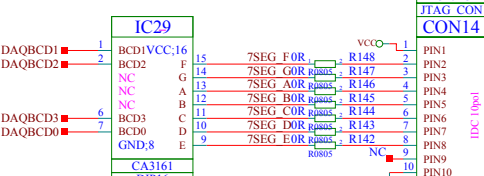
5mm
5mm



to MAN72A seven segment display

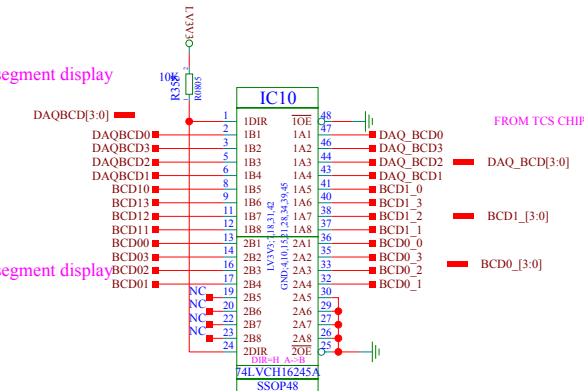


to MAN72A seven segment display

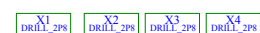


to MAN72A seven segment display

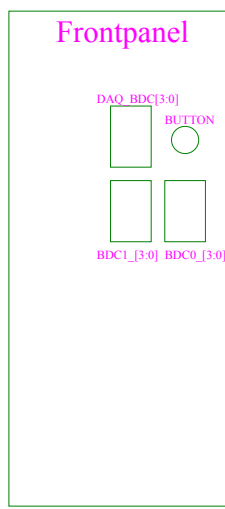
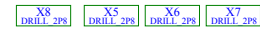
BCD1[3:0]
BCD0[3:0]



Between Virtex2 and 5Volt -7segment driver



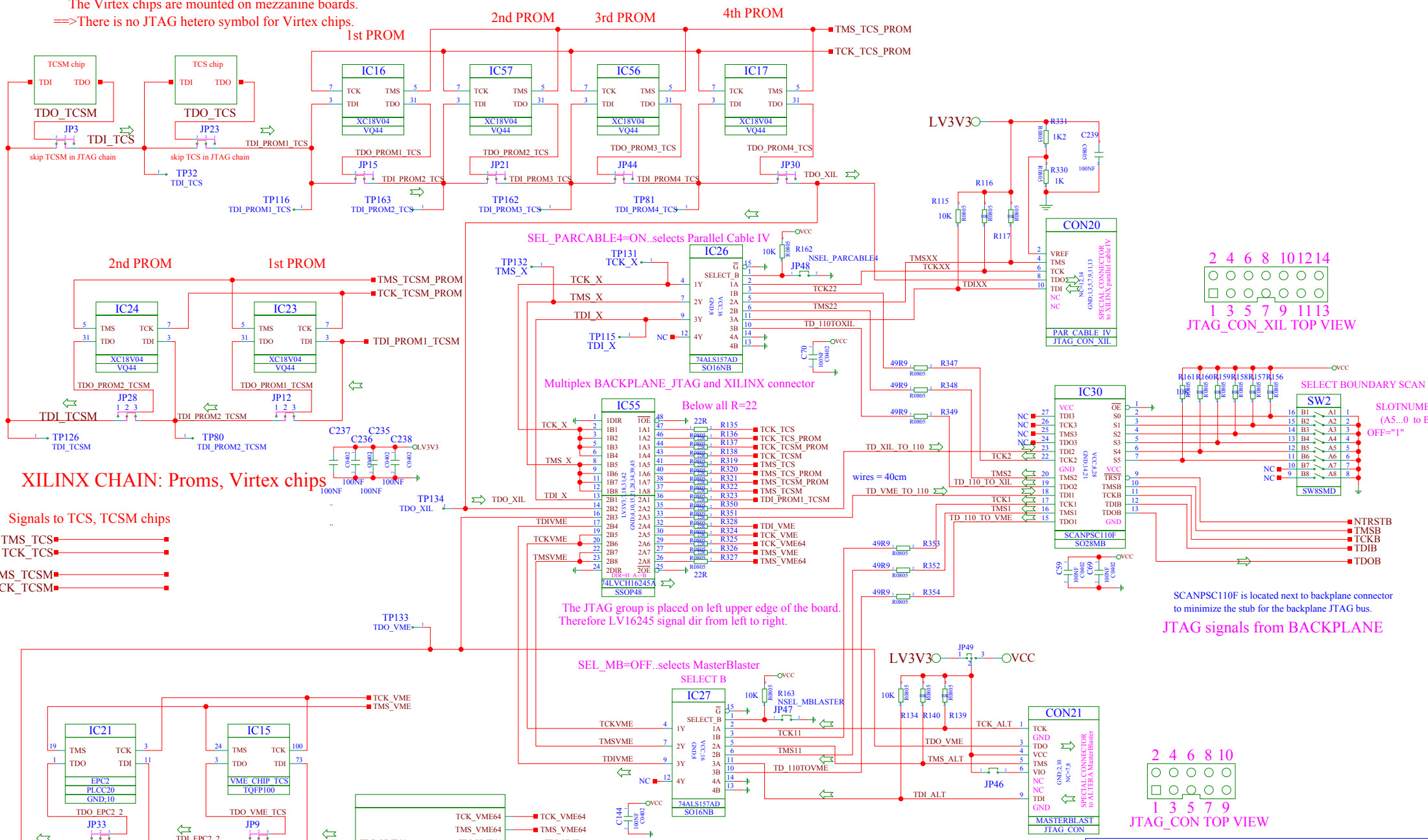
Mounting Holes



TCS-CARD-9U FRONTPAN TCS

HEPHY VIENNA ELEKTRONIK I	sheet 1 of 1
modified by: M.PADRTA	11-13-2003_15:50
checked by: A.TAUROK	23.10.03

The Virtex chips are mounted on mezzanine boards.
 ==>There is no JTAG hetero symbol for Virtex chips.



XILINX CHAIN: Proms, Virtex chips

- Signals to TCS, TCSM chips
- TMS_TCS
 - TCK_TCS
 - TMS_TCSM
 - TCK_TCSM

The JTAG group is placed on left upper edge of the board.
 Therefore LV16245 signal dir from left to right.

SCANPSCI10F is located next to backplane connector
 to minimize the stub for the backplane JTAG bus.
JTAG signals from BACKPLANE

On the TCS board JTAG is used for device configuration only.
 Altera chips are configured either via backplane-JTAG or Master Blaster.
 Xilinx chips are configured either via backplane-JTAG or Parallel Cable IV.
 Both Virtex chips are also configured via VME.

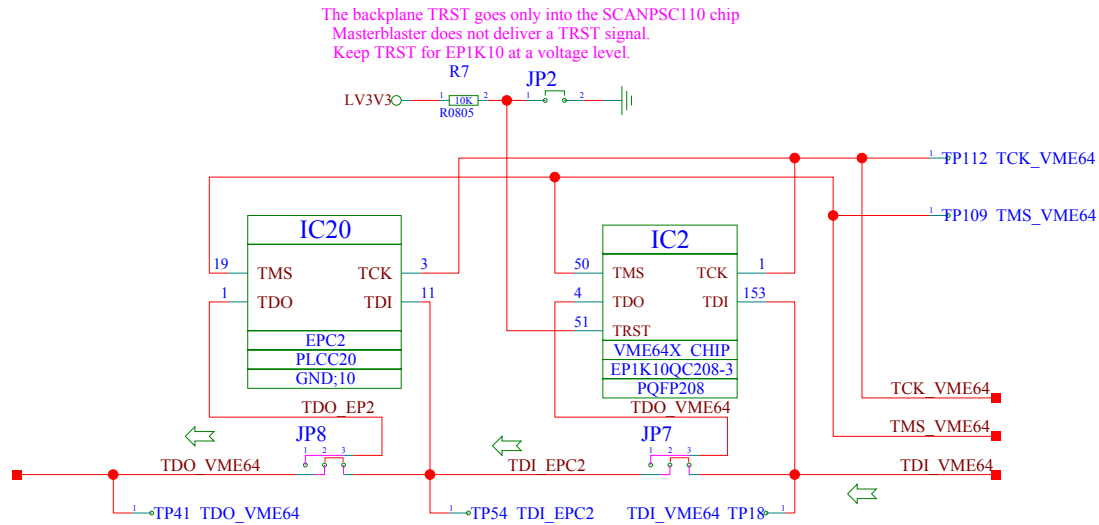
TCS-CARD-9U

JTAG TCS

HEPHY VIENNA ELEKTRONIK I	sheet 1 of 1
modified by: MP, AT	10-28-2003_11:06
checked by: MP+AT	27.10.2003

CHECK if VME64 chip and its PROM have got the same REFDES.

- See schematic 'jtag_vme64x.1'.
- See schematic 'vme_interface.2'.
- See schematic 'vme_interface.3'.

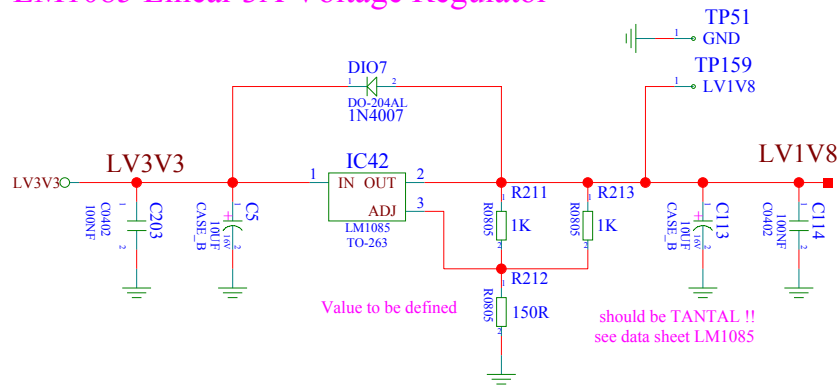


FEHLER: TDO_VME64 bei IC2/4 und bei JP8/2 (HB 200204)

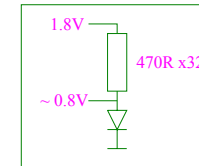
BEHEBUNG: auf Platinen IC2/4 auflöten, Verbindung von aufgelötetem Pin zu TP54 legen. JP7 nicht einlöten. (HB 200204)

<h1>TCS-CARD-9U</h1>	
<h2>JTAG_VME64X</h2>	
HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 1
modified by: HB	2-20-2004_12:06
checked by: A.TAUROK	21.10.2003

LM1085 Linear 3A Voltage Regulator

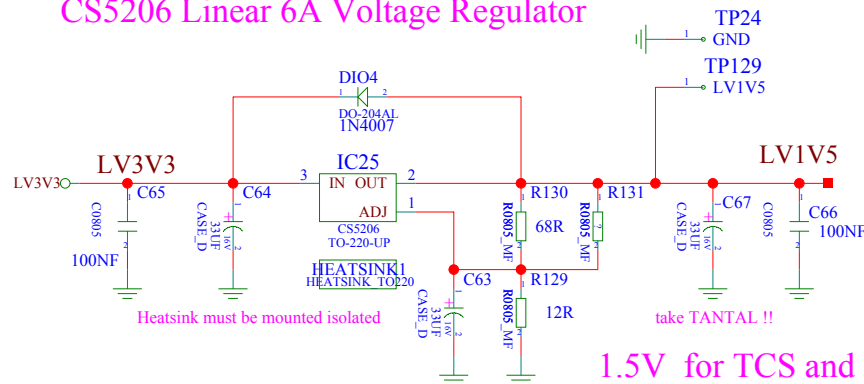


~ 70mA

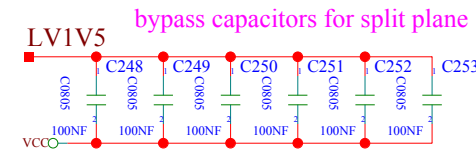


1.8V to bias LVDS input signals from Emulators

CS5206 Linear 6A Voltage Regulator



~ 5A



bypass capacitors for split plane

1.5V for TCS and TCSM chip

V_{ref}

$$(1.240...1.254...1.266)V/68.1 = 18.2...18.4...18.6 \text{ mA} > 10\text{mA}$$

$$250 \text{ mV} / (18.2...18.6 \text{ mA}) = 13.73...13.44 \text{ Ohm}$$

$$\text{Adjust voltage with } R131 = 475...562 \text{ Ohm}$$

$$I_{\text{adj}} = 54 \text{ uA} \dots \text{can be neglected}$$

all resistors for CS5206 in metalfilm

TCS-CARD-9U

POWER_TCS

HEPHY VIENNA
ELEKTRONIK 1

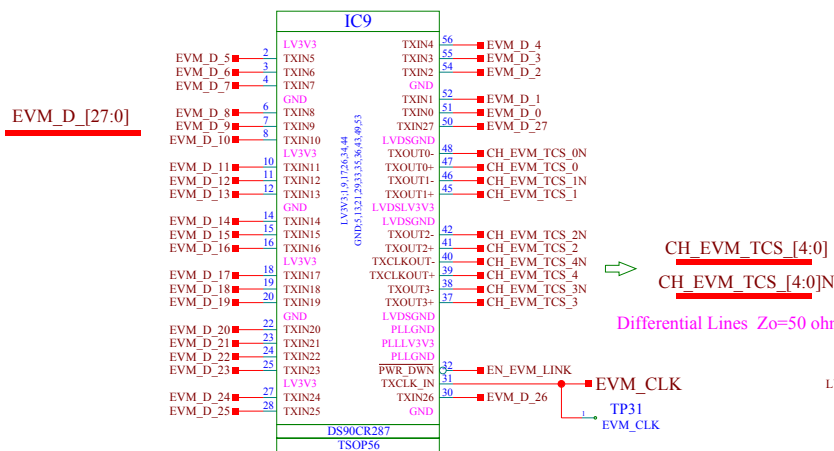
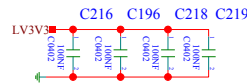
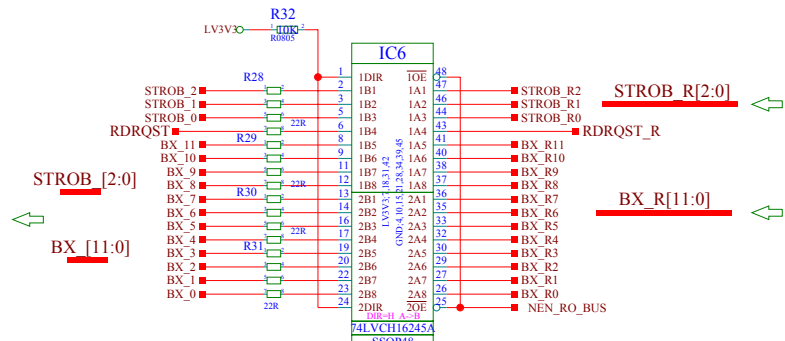
sheet 1 of 1

modified by: M.PADRTA

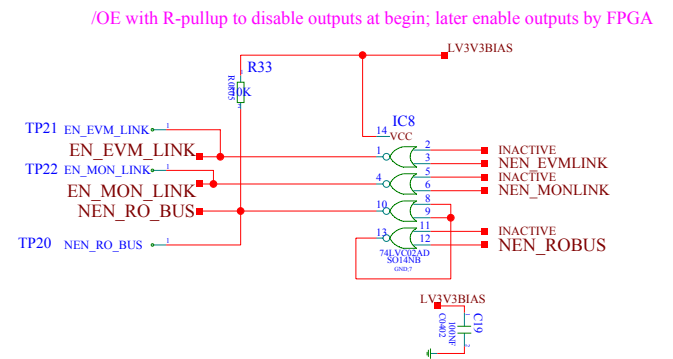
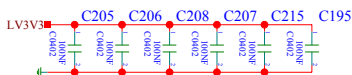
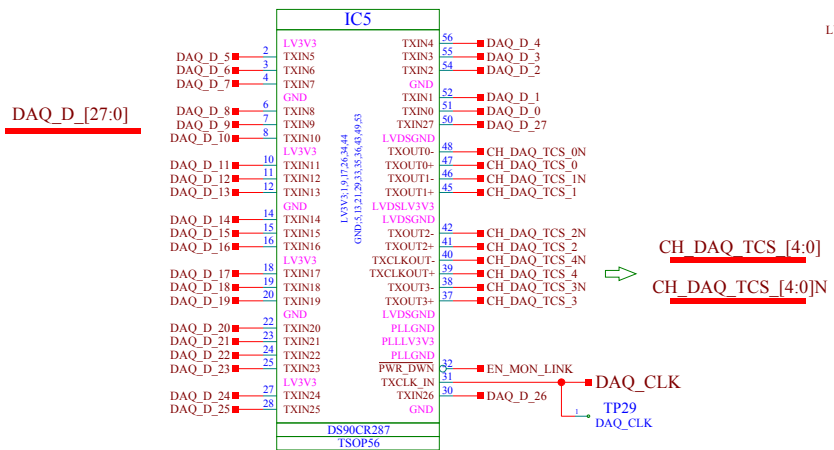
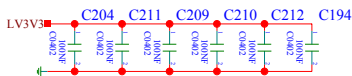
10-28-2003_9:16

checked by: A.TAUROK

17.10.2003



Differential Lines $Z_0=50\text{ ohm} \Rightarrow Z_{diff} \approx 100$



/OE with R-pullup to disable outputs at begin; later enable outputs by FPGA

<h1>TCS-CARD-9U</h1>	
<h2>RO TCS</h2>	
HEPHY VIENNA ELEKTRONIK I	sheet 1 of 1
modified by: A.T	10-27-2003_16:05
checked by: A.TAUROK	21.10.03

DS90CR287 28 bit Channel Link Driver 20-85MHz
DS90CR288A 28 bit Channel Link Receiver 20-85MHz

XC2V1000: 353 min_io +16 clk + prog. + 40 vref pins
 XC2V1500: 441 min_io +16 clk + prog. + 48 vref pins
 XC2V2000: 529 min_io +16 clk + prog. + 56 vref pins

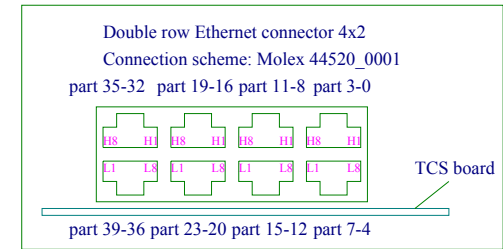
$$Z_{DIFF} = 2 * Z_0 * \left(1 - 0.48.e^{-0.96.s/h} \right) \text{ Ohms}$$

Microstrip (top, bottom) s/h=0.75 : Zdiff= 2*Z₀ * 0.766 smaller distance betw. nets
s/h=1 : Zdiff= 2*Z₀ * 0.816

$$Z_{DIFF} = 2 * Z_0 * \left(1 - 0.347.e^{-2.9.s/h} \right) \text{ Ohms}$$

Stripline (inside) s/h=0.50 : Zdiff= 2*Z₀ * 0.92
s/h=0.75 : Zdiff= 2*Z₀ * 0.96
s/h=1 : Zdiff= 2*Z₀ * 0.98

h = layer thickness
 s = distance between both traces



LVDS over Cable:

Employ ground return wire

LAYOUT RULES for Differential NETS:

LVDS und other CMOS/TTL nets on different planes or separated by 12 mm!!
 or GND trace between

- S = distance between both nets of pair
- >2S = distance between pairs
- >3S = distance to other nets

TRACES: Nach max. 10mm sollen Leitungen parallel laufen.

TRACES: mit immer gleichem Abstand

TRACES: Keine 90 Grad Ecken, die Impedanzsprünge bewirken!!

TRACES: Ecken abrunden or 45 Grad Ecken

TRACES: Stubs <12mm

TRACES: minimize skew

Termination R: distance to pins should be <7mm (max <12mm)

TRACES to GND, Power, C breit und kurz mit vielen Vias (mindestens je 2 Vias)

Driver and Receiver chips nahe dem Stecker platzieren!!

Do not connect unused Receiver pins ==> out =H

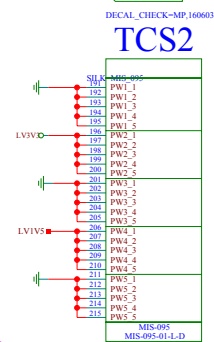
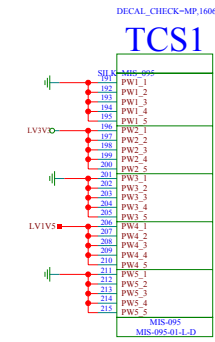
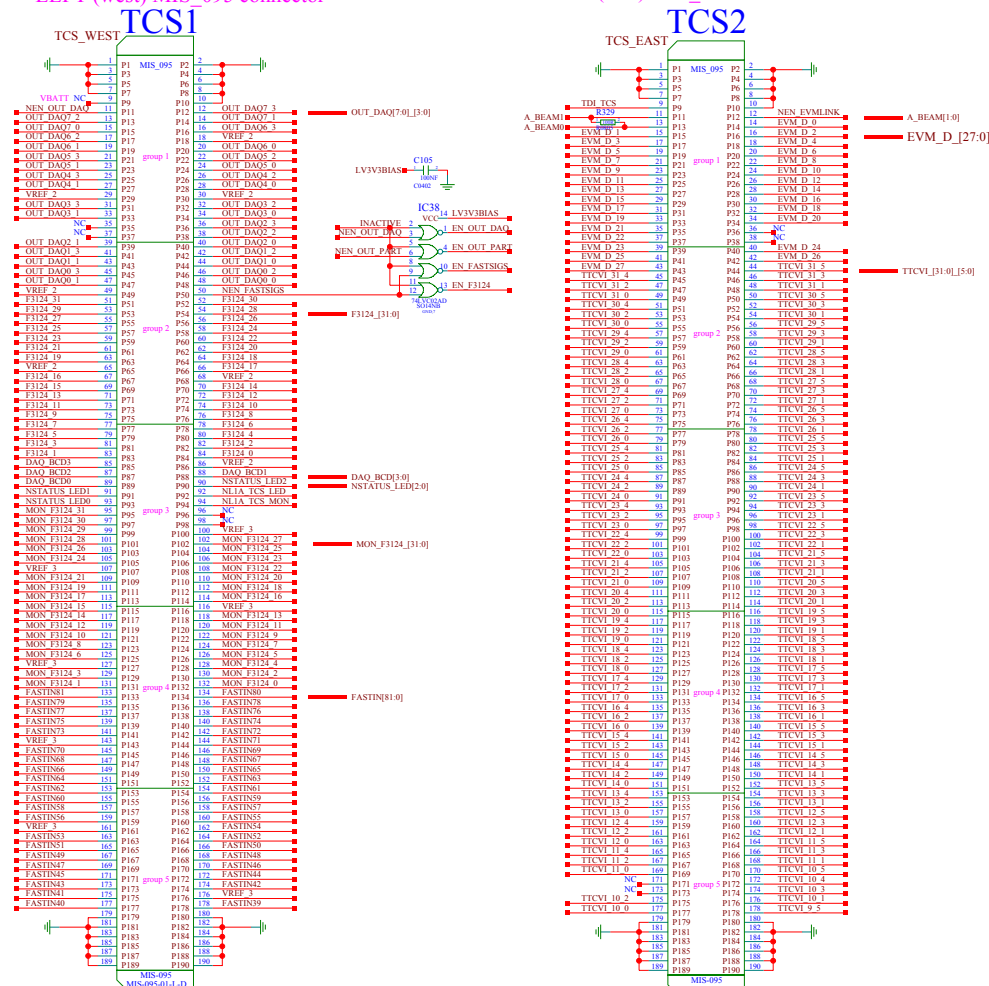
connect unused Driver input pins (LVTTTL side) to GND or Power

Oszi Tastspitze mit >100kOhm/>0.5pF

Oszi Tastspitze mit >100kOhm/>0.5pF

LEFT (west) MIS_095 connector

RIGHT (east) MIS_095 connector



POWER and GND BLADES of MIS connectors

TCS-BOARD-9U TCS CHIP

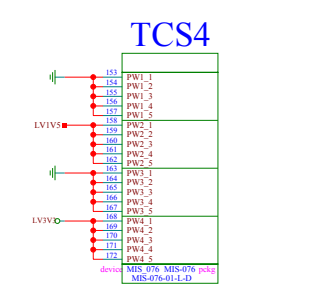
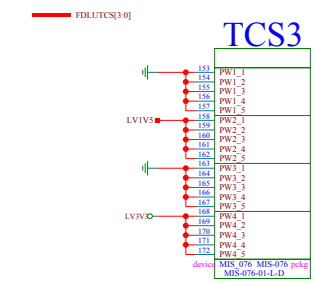
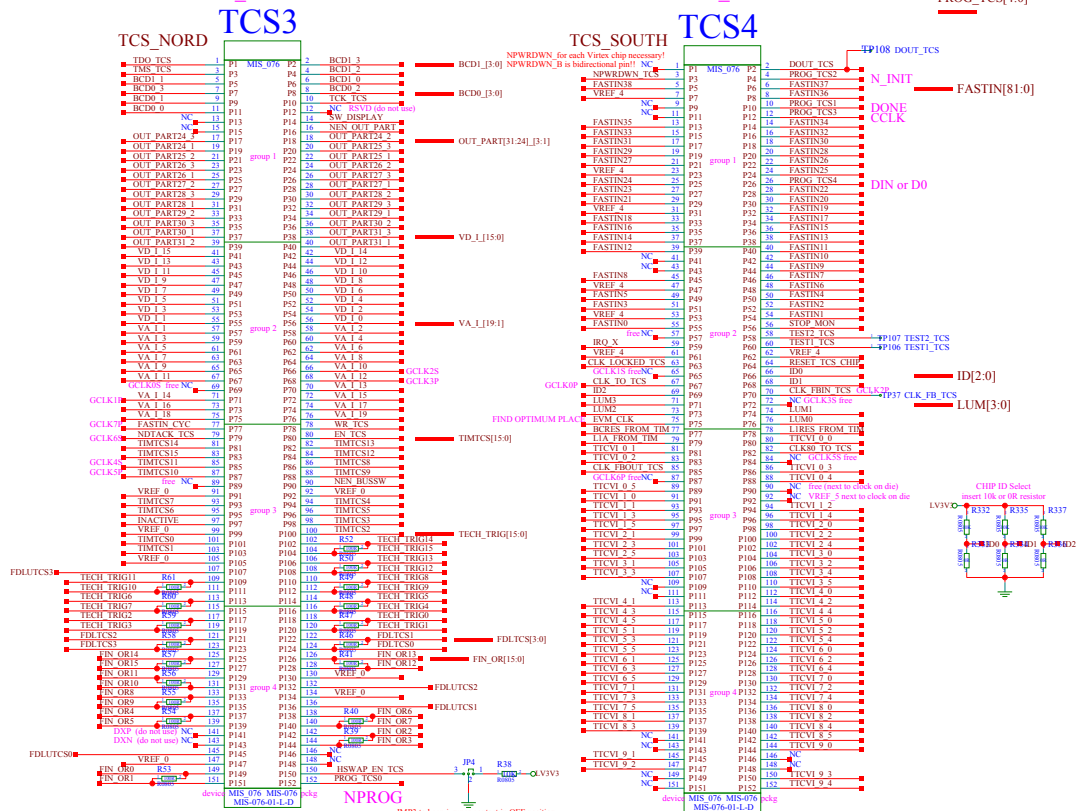
HEPHY VIENNA ELEKTRONIK 1 sheet 1 of 3

modified by: M.PADRITA 10-30-2003_11:00

UPPER MIS_076 connector

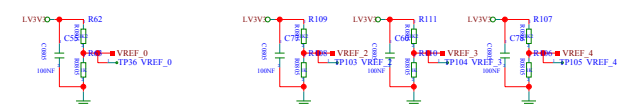
LOWER MIS_076 connector

din_cclk_mnit_dino_nprog
PROG_TCS[4:0]



VREF for TCS Chip Banks 0,2-4

einige freie Pins auf Testpunkte legen



keep Vref for FASTIN signals (Bank3 & 4)

TCS-BOARD-9U

TCS CHIP

HEPHY VIENNA ELEKTRONIK 1 sheet 2 of 3

modified by: M.PADRTA 10-30-2003_11:00

checked by: MP+AT 30.10.2003

Do not change Refdes for Virtex (used for automatic checks)

LOGIC IDEEN:

to EVM: raw Algos of 1 bx
to DAQ: raw Algos of 3(5) bx

RATE COUNTER monitoring

192 counters 32bits

1sec=>40 Mio=262 5A00

6 sec =E4...=28 bits

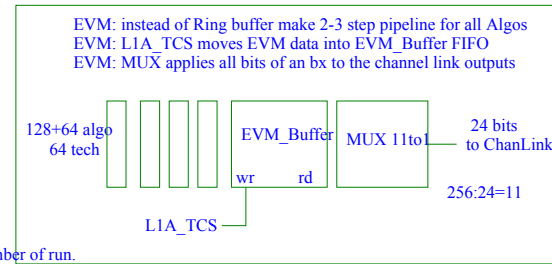
107 sec =E4...=32bits

Reset Rate counters every 1 sec or 10 sec

The reset stores all counters into registers.

The reset stores also the overall orbit number

FDL: decodes Reset Orbit instruction to get overall orbit number of run.



TIMTCS[15:8] TCS-to-TIM
LIA_FROM_TCS
14:8 undefined

TIMTCS[7:0] TIM-to-TCS
TIM_ERR maybe combine to 1 signal
TIM_OUT_OF_SYNC
TIM_WARNING_OVFLO
TIM_READY

TIM_BUSY
LI_RES also sent as lvds signal: RESET
TI_INHIBIT_PHYS_LIA how to use it??
TI_INHIBIT_ALL_LIA how to use it??

XC2Vxxx-4...slower, -5...faster version

XC2V2000-4FG676 456 io XC2V2000-4FF896 624 io; delivery time ~8 weeks (May02)
XC2V1500-4FG676 392 io XC2V1500-4BG575 392 io XC2V1500-4FF896 528 io; delivery starting Nov02
XC2V1000-4FG456 324 io XC2V1000-4BG575 328 io XC2V1000-4FF896 432 io; delivery time ~5 weeks (May02)

Device	Row x Col	/Slices/RAM kbits/Multiplier/RAMBlocks (Kbits)/DCMs/maxIO pads
XC2V1000	40x32	5120 160 40 40 8 432
XC2V1500	48x40	7680 240 48 48 8 528

XC2V1000: =10240 DFF
XC2V1500: =15360 DFF

1slice= F+G LUT, 2 FF, hor.cascade OR,

Monitor RAMs: (192+16+68)/16 = 18RAMBlocks RingBuf (DPM)
18RAMBlocks RC-Buf (Fifo)
18RAMBlocks BX-Buf
18RAMBlocks L1-Queue

RI-BUF VME-access: A15-A1 for 18 1kW-DPMs

FDL chip pins: 369 (without ALGO bits to EVM)

Algo bits to Event Manager:

~~Option1: Send Algo bits to FDL chip and to output drivers ==> NOT enough pins on TCS com~~

Option2: LIA extracts data from RI-buf and sends them via ChanLink to EVM-link

Option2: ...and via another ChanLink to GTPE

Option2: 369 + 30 pins too many for chip ==> reduce other pins

Monitor: not prescaled algo bits

RATE counters: prescaled algo bits

TCS ==> FDL: LIA for EVM readout

TCS I/O pins: 38+33+192+30+3 +2+24+33+96(xx)= 451
355 +24 (8ser)=379

MIS...mounted on TCS board
MIT...mounted on mezzanine board

Option:

VIRTEX mit 896 pins auf eine kleine Platine geben:

Vorteil: austauschbar (Reparatur, Upgrade),

Vorteil: Layout mit 150 um und 0.3 vias moeglich

Vorteil: Diese Platine bei FDL und TCS verwendbar

Nachteil: etwas mehr Platzbedarf

Nachteil: Mehrpreis für 50 Ohm bd-bd Stecker

Nachteil: mehr Lötstellen=> fehleranfälliger?

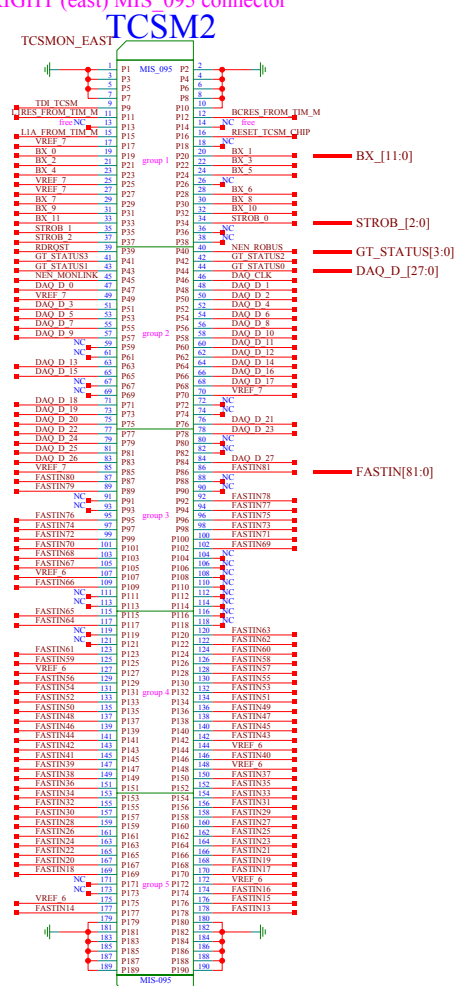
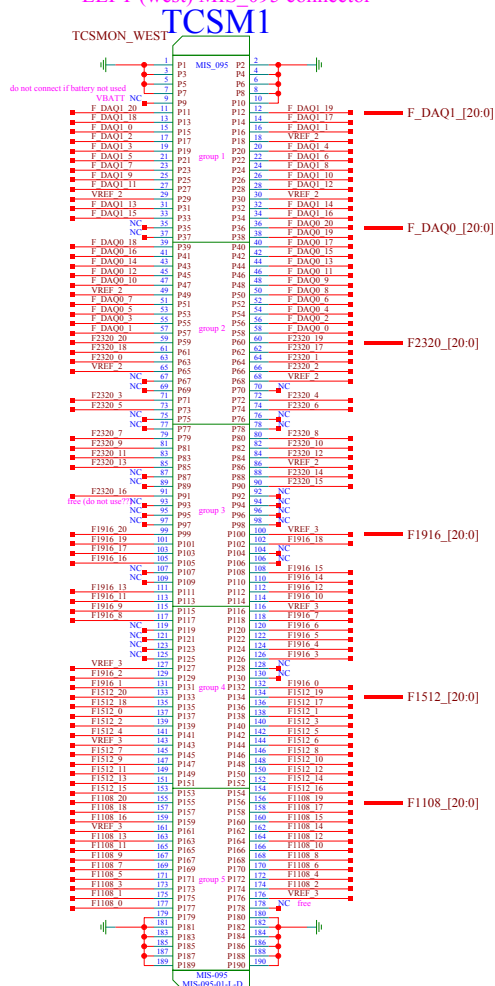
TCS-BOARD-9U

TCS CHIP

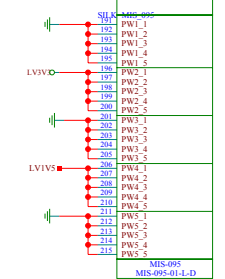
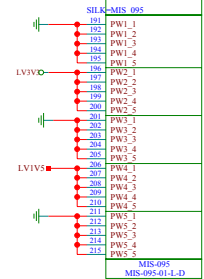
HEPHY VIENNA ELEKTRONIK I	sheet 3 of 3
modified by: M.P.	1-30-2003_14:47
checked by: CHECKER	0-00-0000_00:00

LEFT (west) MIS_095 connector

RIGHT (east) MIS_095 connector



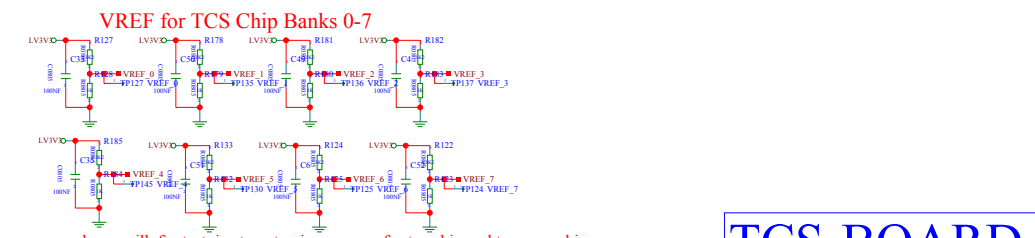
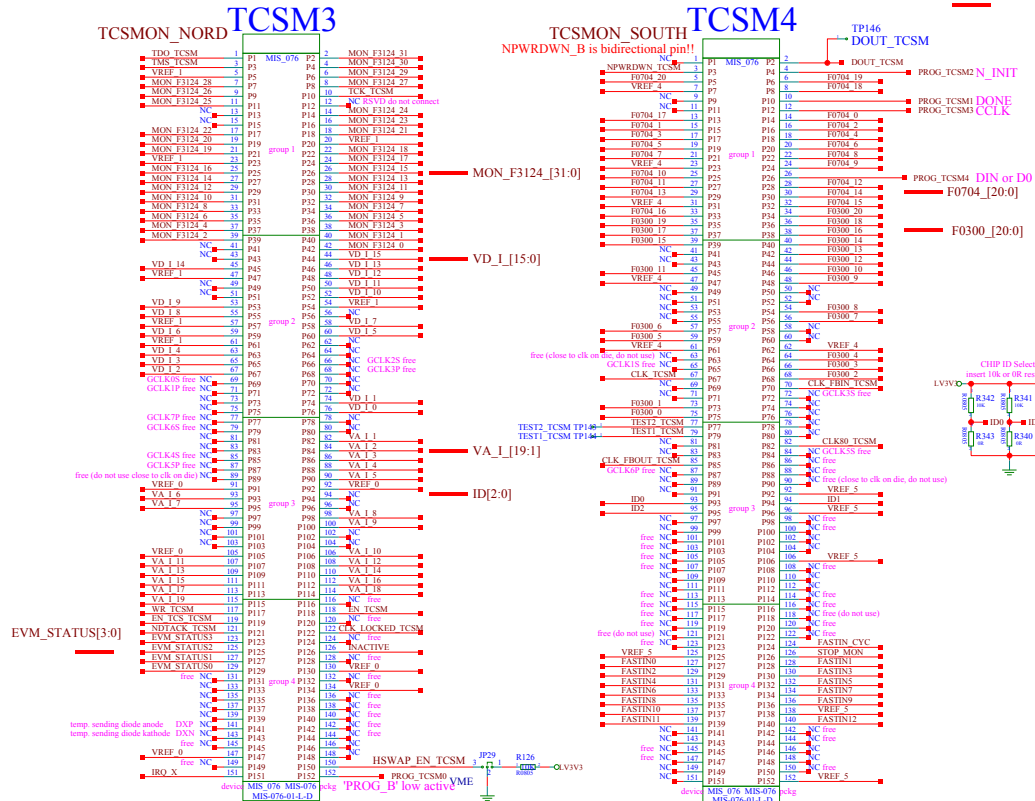
TCSM1 POWER and GND BLADES of MIS connectors



TCS-BOARD-9U
TCS MON CHIP

HEPHY VIENNA ELEKTRONIK 1 sheet 1 of 2

modified by: M.P. 10-30-2003_11:01



change silk for testpins to get unique names for tes-chip and tes-mon-chip

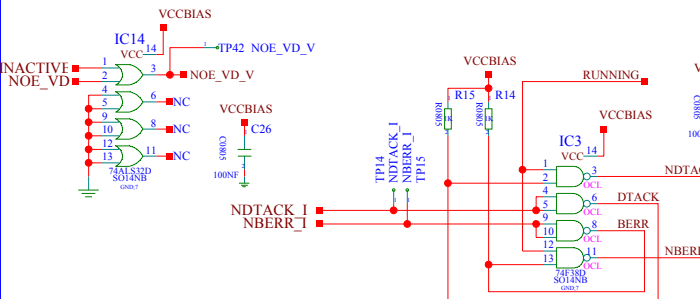
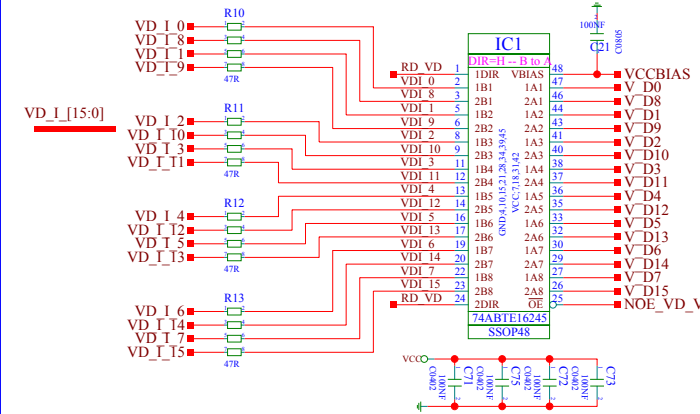
TCS-BOARD-9U TCS MON CHIP

HEPHY VIENNA ELEKTRONIK 1 sheet 2 of 2

modified by: M.P. 10-30-2003_11:01

checked by: AT+MP 30.10.2003

47 Ohm resistors protect the Virtex drivers against overvoltage spikes.



Keep NDTACK NBERR inactive while VME64X chip is unconfigured

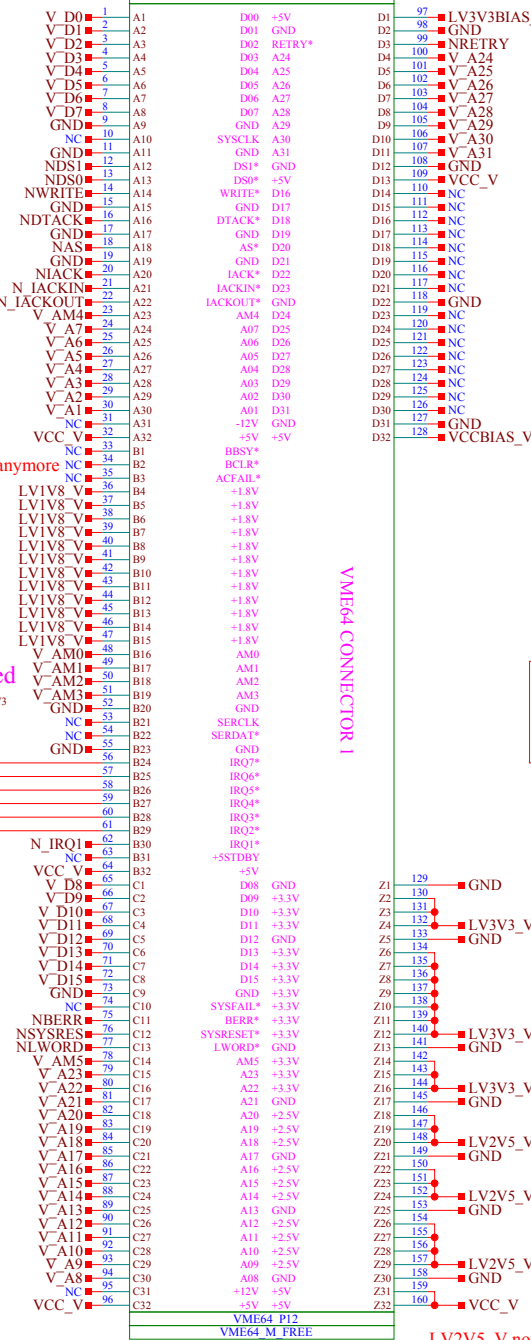
TSC9U mounted in SLOT 7

SLOT: NGAP NGA4 NGA3 NGA2 NGA1 NGA0
 SLOT7: Open Open Open GND GND GND

Geographical Addresses inverted values

Parity bit: for odd parity
 slot=1: GA=0 0001 => GAP=0
 slot=2: GA=0 0010 => GAP=0
 slot=3: GA=0 0011 => GAP=1
 etc

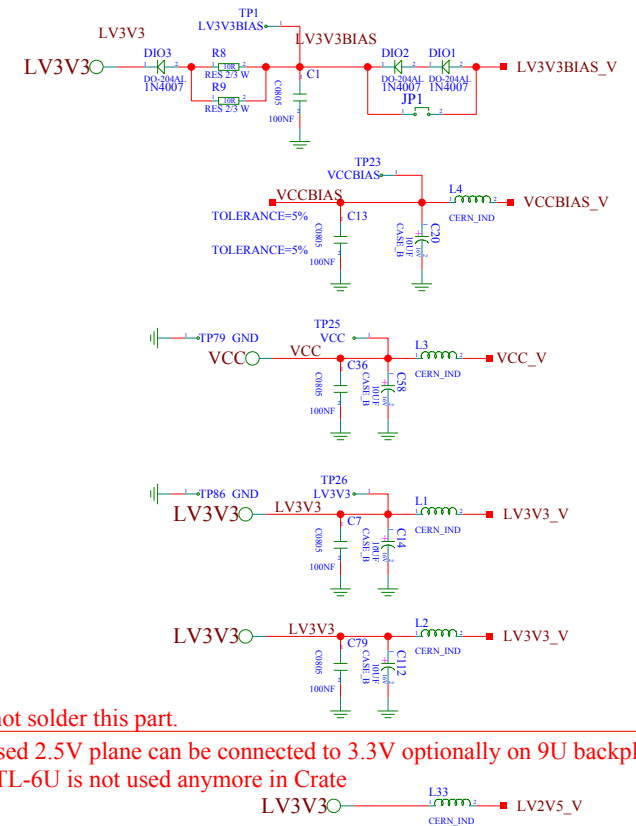
See VME64x.pdf page 10 Table 3-2



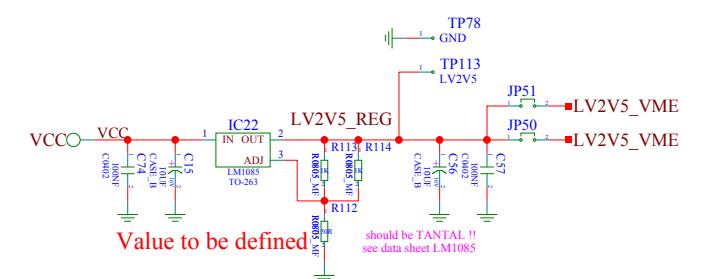
VME64 CONNECTOR 1

LV2V5_V not used anymore

for 9U backplane remove DIO1 and DIO2 and solder JP1
 for 6U backplane insert DIO1 and DIO2; JP1 = open
 LV3V3BIAS_V is at VCC in GT-6U-backplane!



Do not solder this part.
 Unused 2.5V plane can be connected to 3.3V optionally on 9U backplane if GTL-6U is not used anymore in Crate



TCS9U does not use LV2V5 and LV1V8 from BACKPLANE-6U
 LV2V5 and LV1V8 are not provided by the Backplane-9U

TCS-CARD-9U

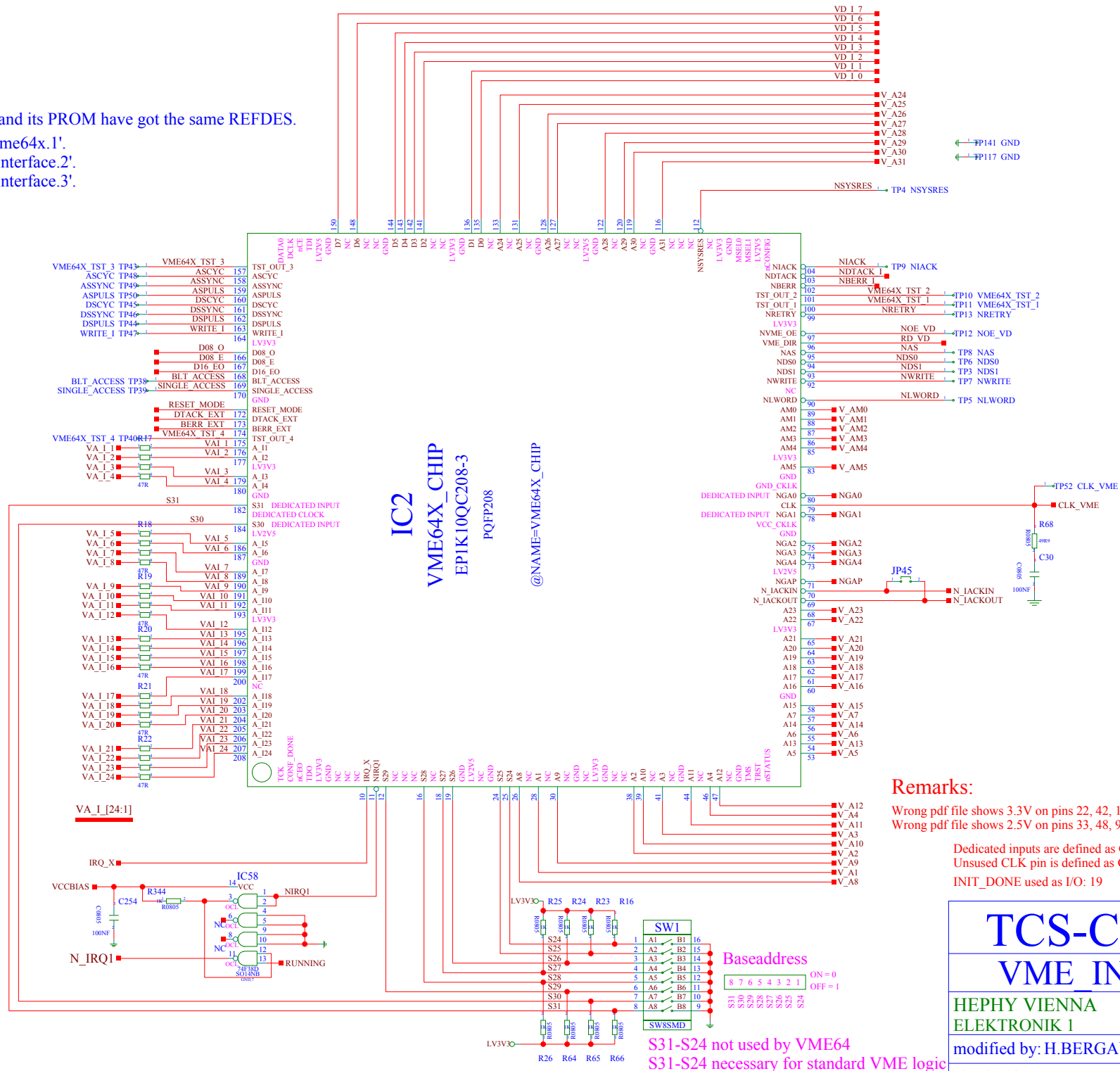
VME INTERFACE

HEPHY VIENNA ELEKTRONIK I	sheet 1 of 3
modified by: H. BERGAUER	10-28-2003_11:00
checked by: A TAUROK	8-18-2003_16:53

Stecker und Signale mit GTL und TIM schematic vergleichen

CHECK if VME64 chip and its PROM have got the same REFDES.

See schematic 'jtag_vme64x.1'.
 See schematic 'vme_interface.2'.
 See schematic 'vme_interface.3'.

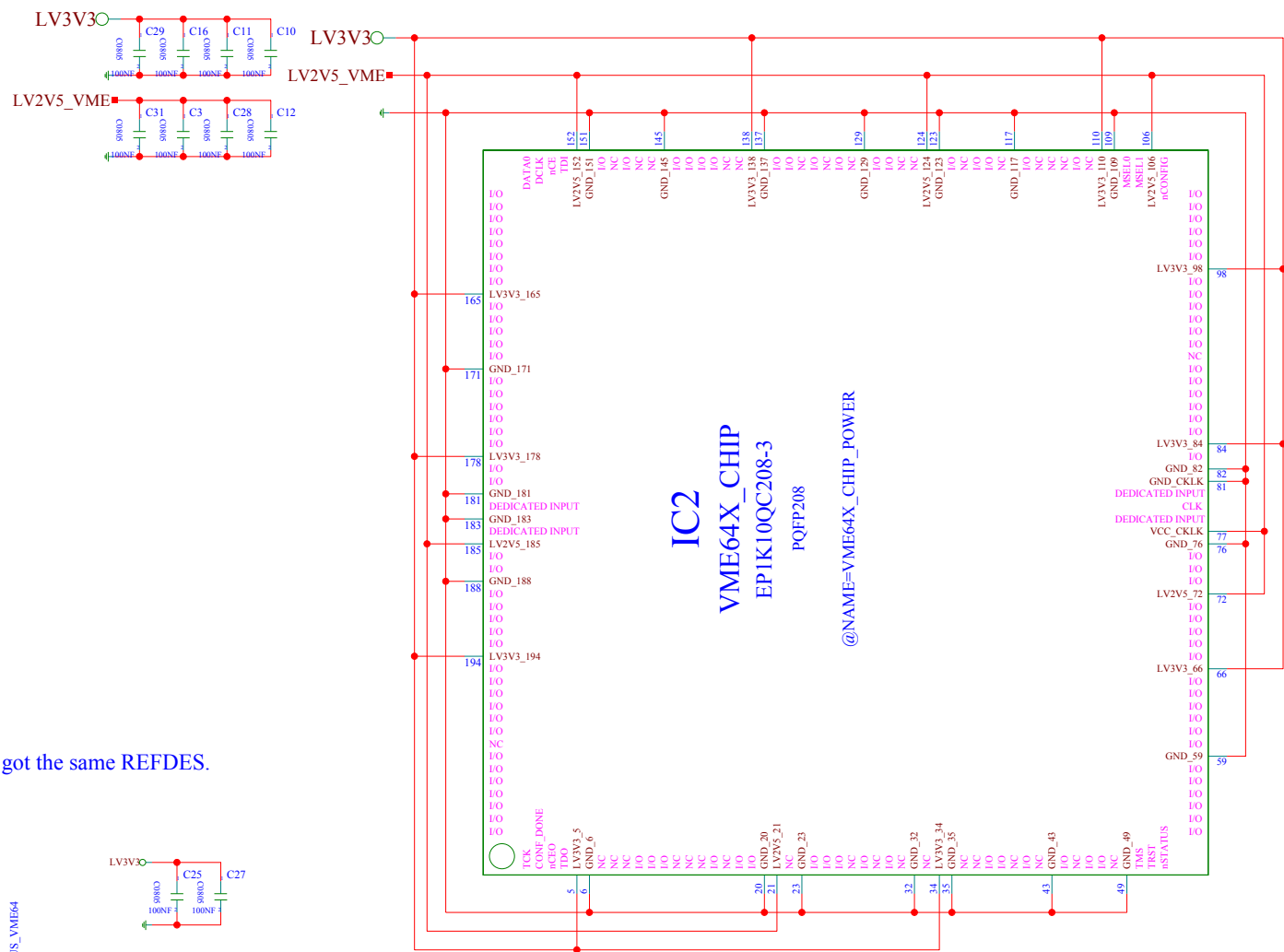


Remarks:

- Wrong pdf file shows 3.3V on pins 22, 42, 118, 146. See PIN file for reference.
- Wrong pdf file shows 2.5V on pins 33, 48, 91, 130, 201. See PIN file for reference.
- Dedicated inputs are defined as GND: 78 80 182 184
- Unused CLK pin is defined as GND: 183
- INIT_DONE used as I/O: 19

S31-S24 not used by VME64
 S31-S24 necessary for standard VME logic

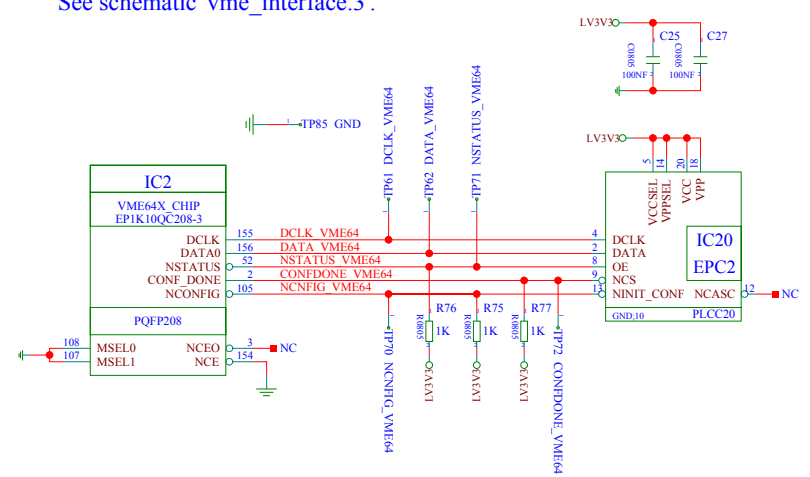
<h1>TCS-CARD-9U</h1>	
<h2>VME INTERFACE</h2>	
HEPHY VIENNA ELEKTRONIK I	sheet 2 of 3
modified by: H.BERGAUER	10-21-2003_16:03
checked by: A.TAUROK	21.10.2003



This pin is the power or ground for the ClockLock and ClockBoost circuitry of a PLL. To ensure noise resistant the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device.
If the PLL is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.

CHECK if VME64 chip and its PROM have got the same REFDES.

- See schematic 'jtag_vme64x.1'.
- See schematic 'vme_interface.2'.
- See schematic 'vme_interface.3'.



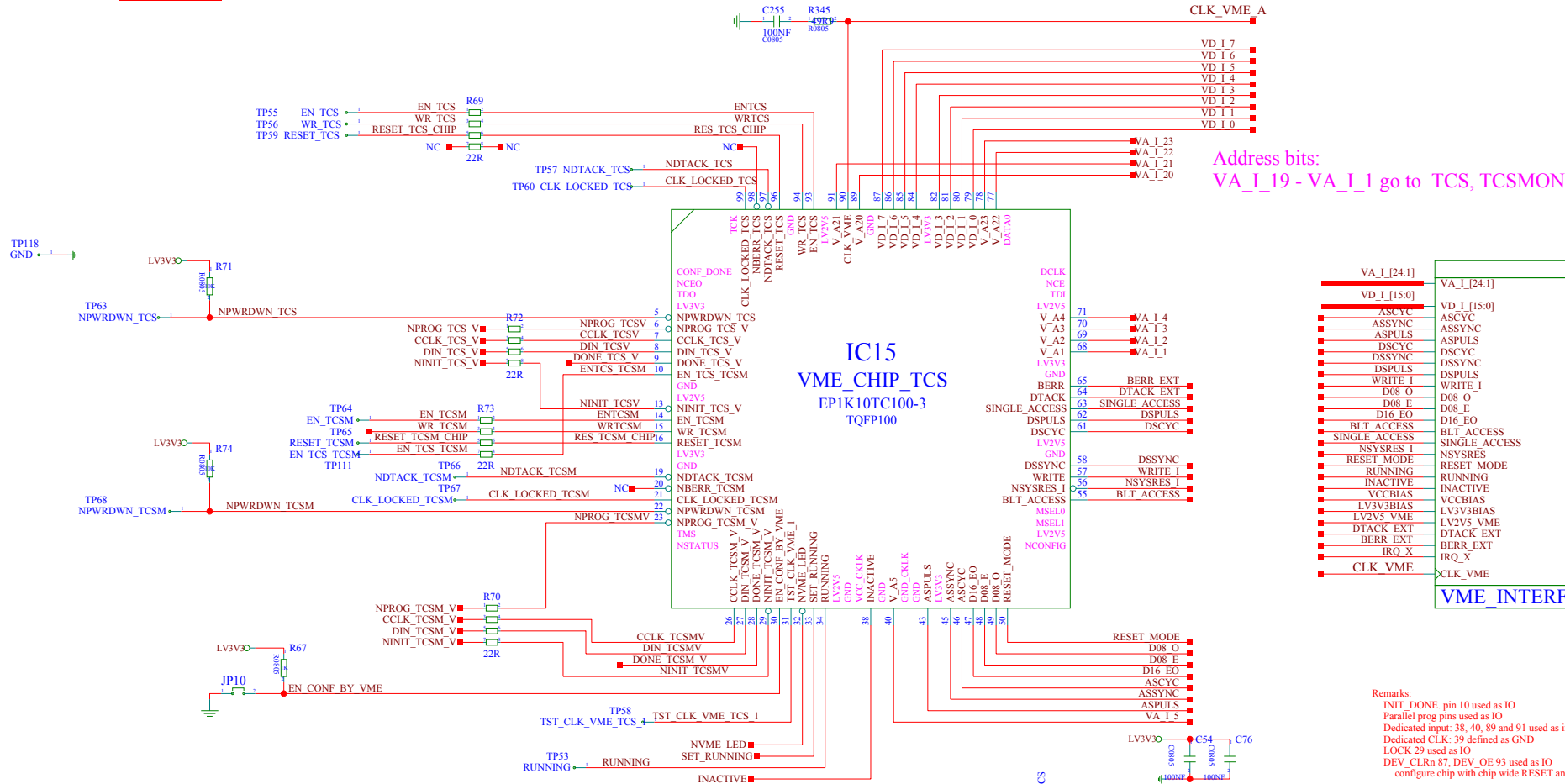
A.T. Aug03: See configdevices.pdf.
Do not insert R75, R76, R77 when internal pullup R are used in IC20: EPC2
All pull-up resistors are 1 k.

TCS-CARD-9U VME INTERFACE

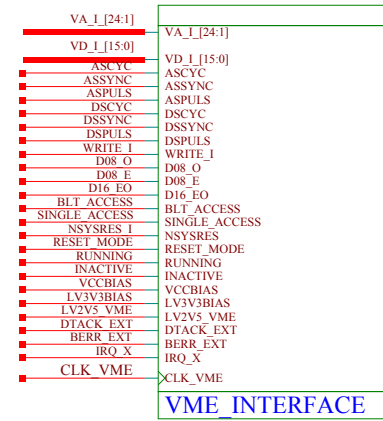
HEPHY VIENNA ELEKTRONIK 1	sheet 3 of 3
modified by: H. BERGAUER	10-27-2003_10:23
checked by: A.TAUROK	21.10.2003

VA_I_[19:1]

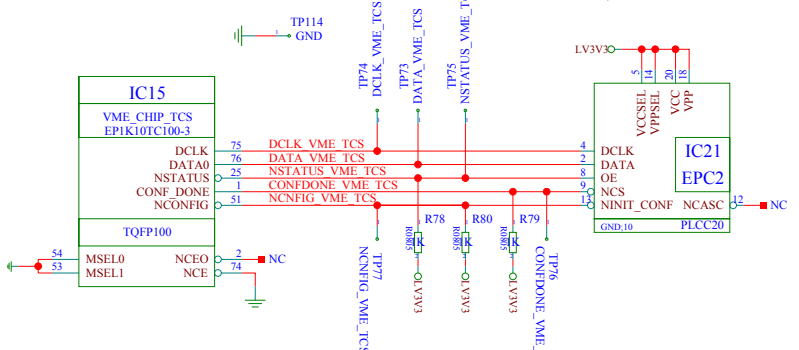
R und C voerst nicht einlöten.



Address bits:
VA_I_19 - VA_I_1 go to TCS, TCSMON



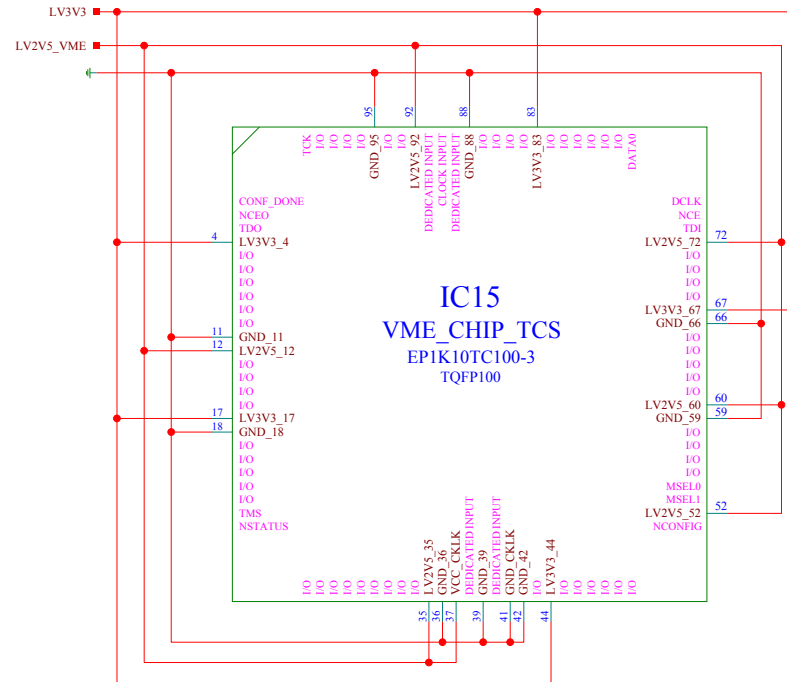
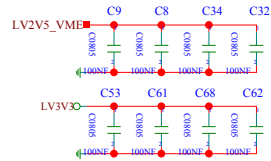
Remarks:
INIT_DONE. pin 10 used as IO
Parallel prog pins used as IO
Dedicated input: 38, 40, 89 and 91 used as input
Dedicated CLK: 39 defined as GND
LOCK 29 used as IO
DEV. CLRn 87, DEV. OE 93 used as IO
configure chip with chip wide RESET and 3-state options



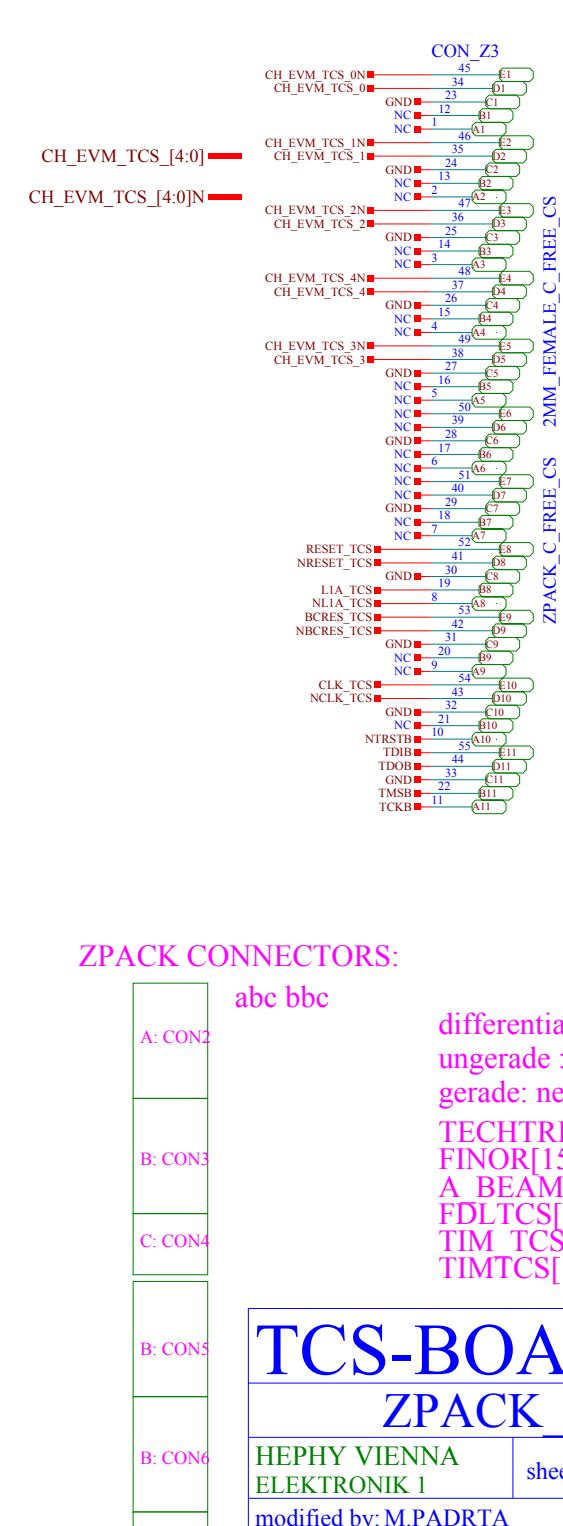
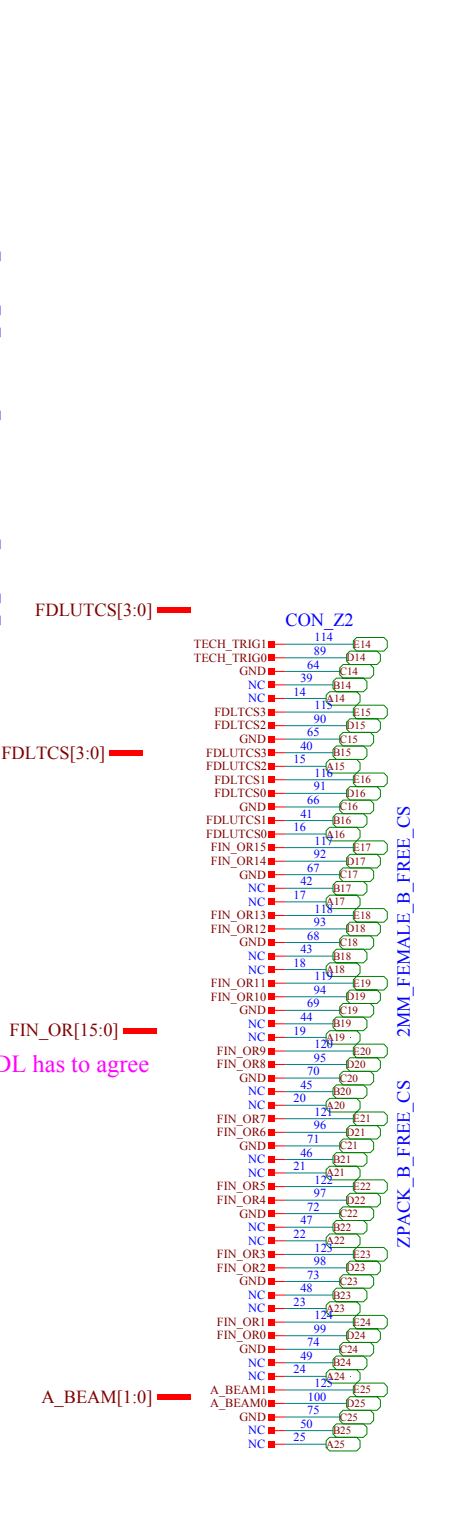
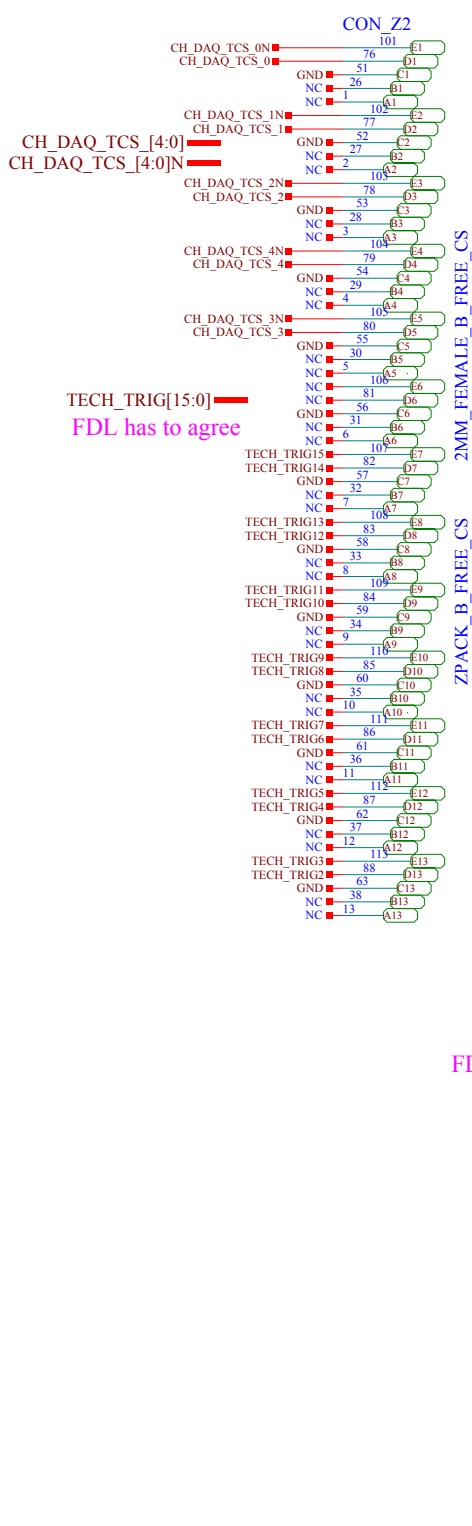
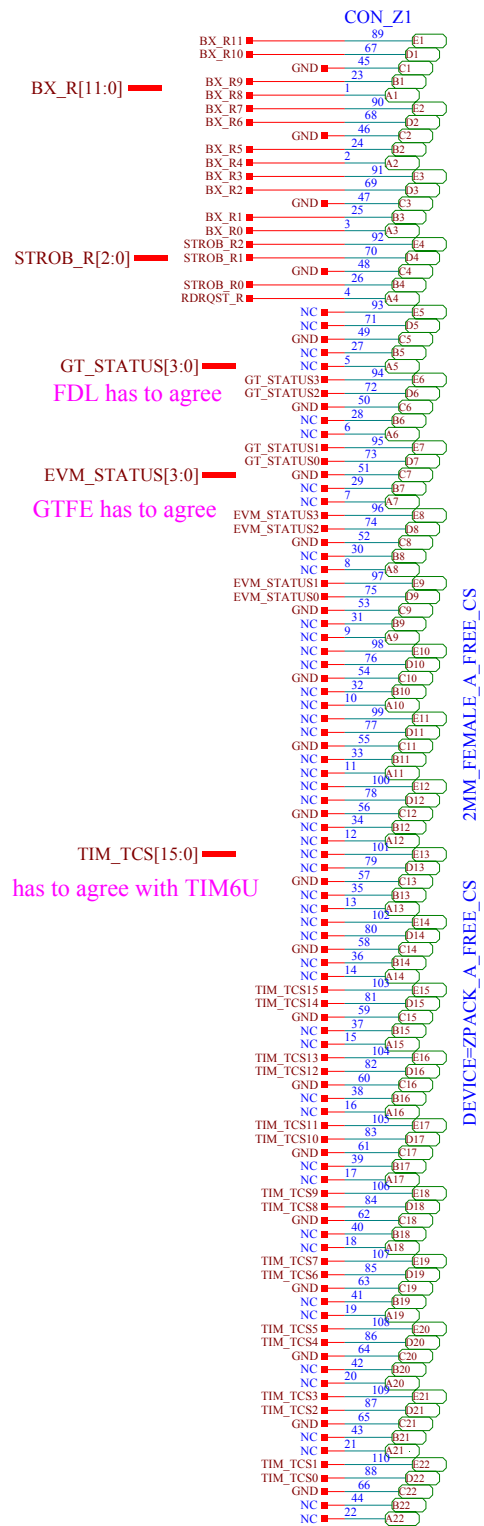
A.T. Aug03: See configdevices.pdf.
Do not insert R78, R79, R80 when internal pullup R are used in IC21: EPC2
All pull-up resistors are 1 k.

Checked by AT 18.Aug 03
Herbert will kein Chip ID

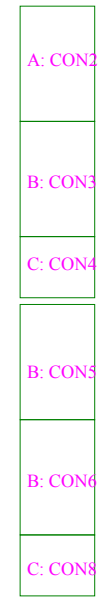
<h1>TCS-CARD-9U</h1>	
<h2>VME IO TCS</h2>	
HEPHY VIENNA ELEKTRONIK I	sheet 1 of 2
modified by: M.PADRTA	1-7-2004_16:14
checked by: HB+AT	27.10.03



<h1>TCS-CARD-9U</h1>	
<h2>VME IO TCS</h2>	
HEPHY VIENNA ELEKTRONIK 1	sheet 2 of 2
modified by: M.PADRTA	10-27-2003_10:43
checked by: AT+HB	27.10.03



ZPACK CONNECTORS:



abc bbc
 differential signals
 ungerade : positive
 gerade: negative

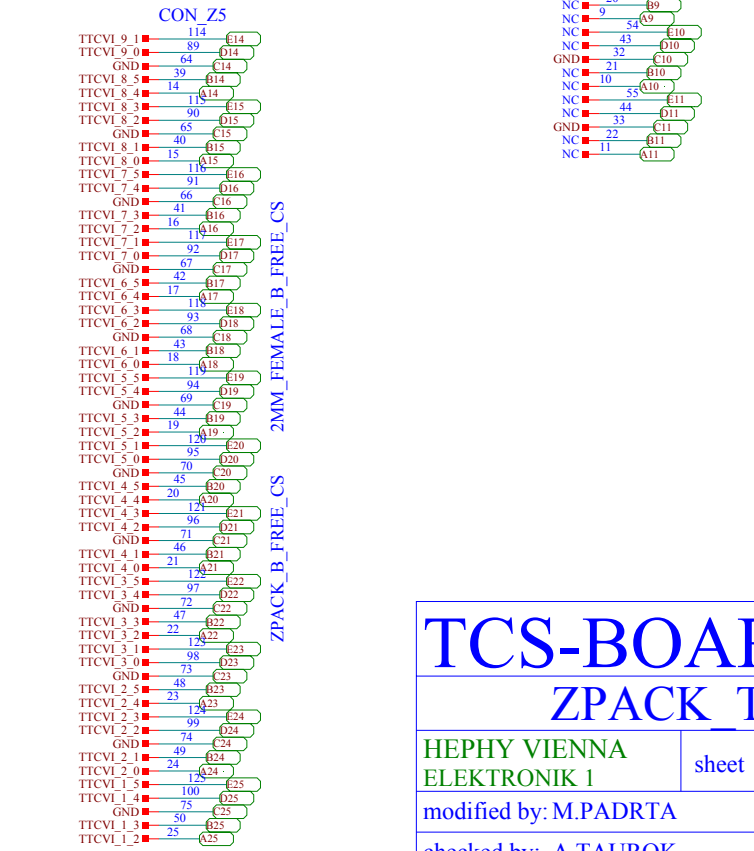
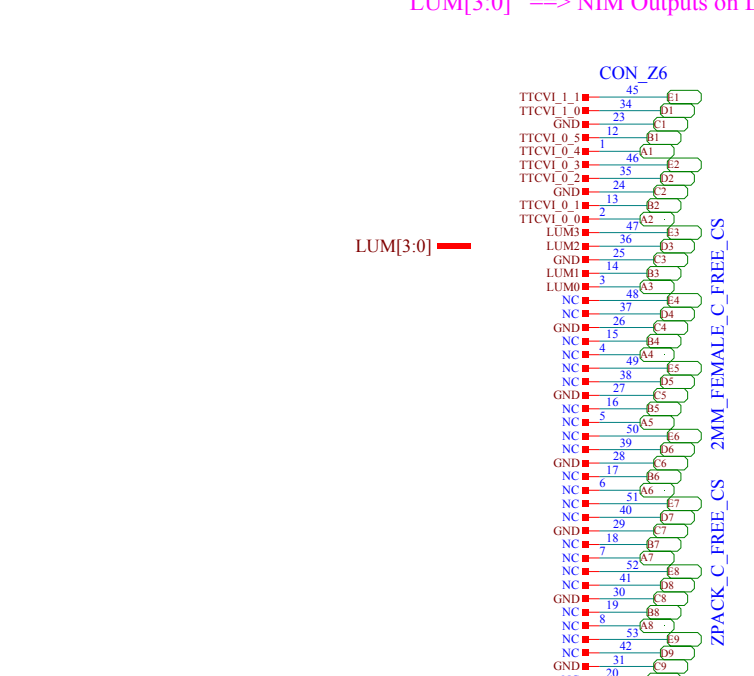
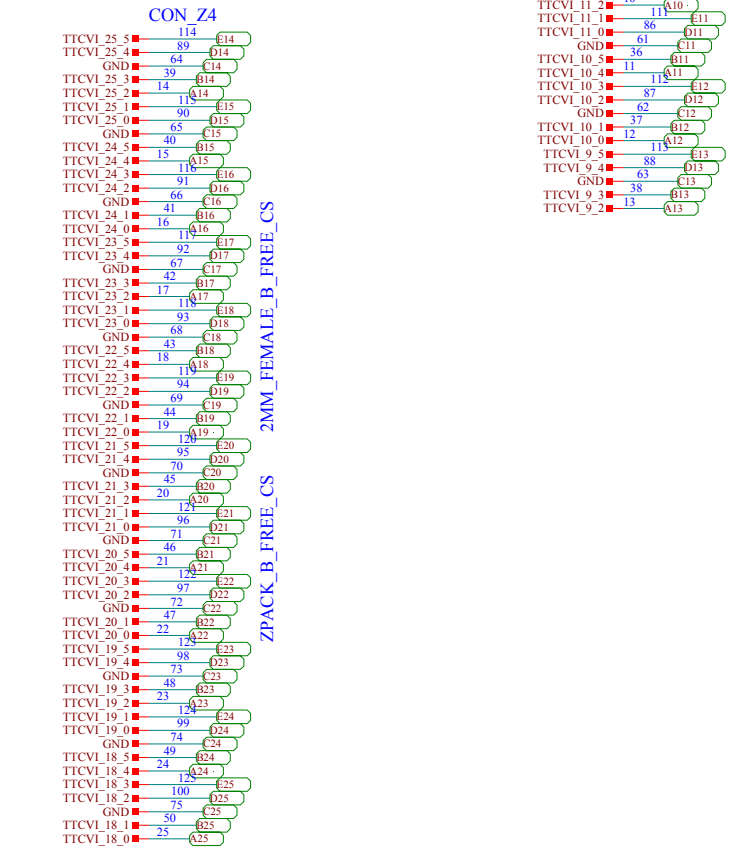
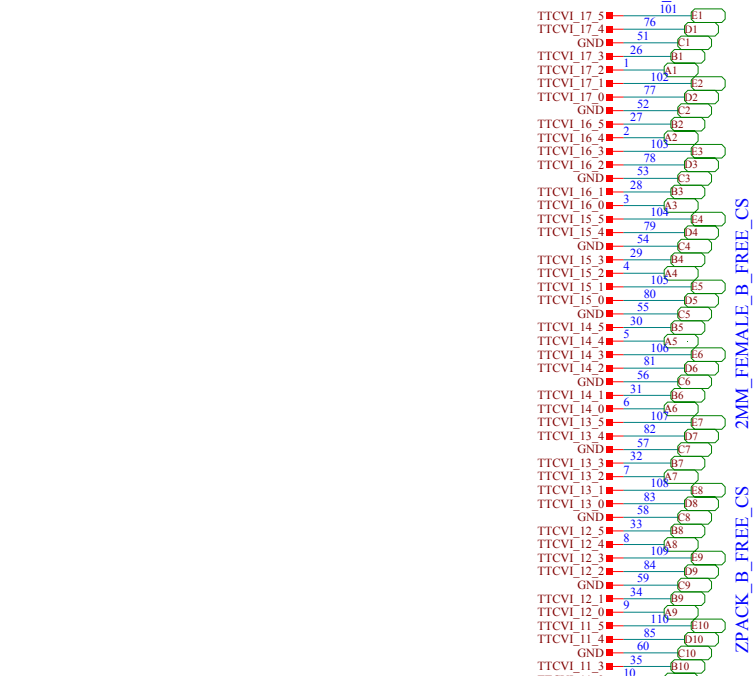
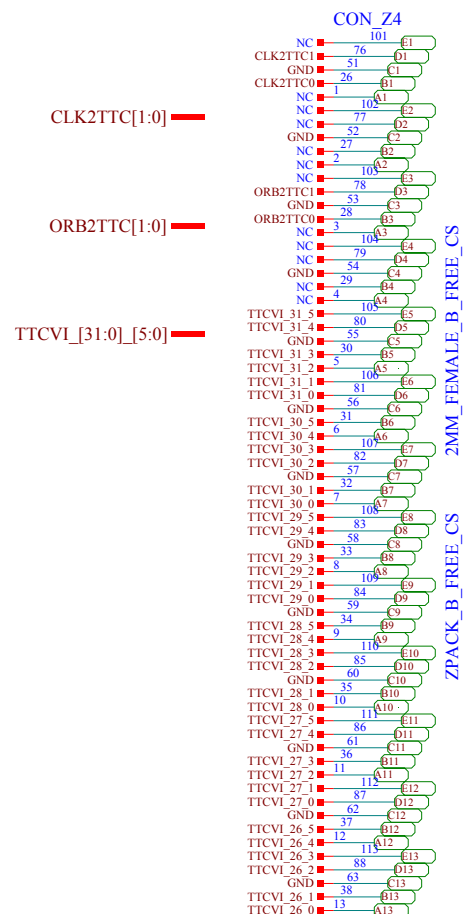
TECHTRIG[15:0]
 FINOR[15:0]
 A_BEAM[1:0]
 FDLTCS[3:0]
 TIM_TCS[15:0]
 TIMTCS[15:0]

TCS-BOARD-9U

ZPACK TCS

HEPHY VIENNA ELEKTRONIK I	sheet 1 of 2
modified by: M.PADRITA	10-27-2003_18:15
checked by: A.TAUROK	24.10.03

TCS9U has been moved to Slot7 and receives now BX_L[11:0]...



TCS-BOARD-9U	
ZPACK TCS	
HEPHY VIENNA ELEKTRONIK I	sheet 2 of 2
modified by: M.PADRTA	10-27-2003_18:17
checked by: A.TAUROK	24.10.03