

Declarations**Ports:**

```

A_BEAM          : std_logic_vector(1 DOWNT0 0)
BCRES_FROM_TIM : std_logic
CLK80_TO_TCS   : std_logic
CLK_FBIN_TCS   : std_logic
CLK_TO_TCS     : std_logic
EN_TCS         : std_logic
F3124          : std_logic_vector(31 DOWNT0 0)
FASTIN         : std_logic_vector(81 DOWNT0 0)
FASTIN_CYC     : std_logic
FDLTCS_L       : std_logic_vector(1 DOWNT0 0)
FDLUTCS_L      : std_logic_vector(1 DOWNT0 0)
FIN_OR         : std_logic_vector(15 DOWNT0 0)
ID             : std_logic_vector(2 DOWNT0 0)
INACTIVE       : std_logic
L1A_FROM_TIM   : std_logic
L1RES_FROM_TIM : std_logic
RESET_TCS_CHIP : std_logic
SW_DISPLAY     : std_logic
TECH_TRIG      : std_logic_vector(15 DOWNT0 0)
TIMTCS_L       : std_logic_vector(7 DOWNT0 0)
VA_I           : std_logic_vector(19 DOWNT0 1)
WR_TCS         : std_logic
BCD0           : std_logic_vector(3 DOWNT0 0)
BCD1           : std_logic_vector(3 DOWNT0 0)
CLK_FBOU_TCS  : std_logic
CLK_LOCKED_TCS : std_logic
DAQ_BCD        : std_logic_vector(3 DOWNT0 0)
EVM_CLK        : std_logic
EVM_D          : std_logic_vector(27 DOWNT0 0)
FDLTCS_H       : std_logic_vector(1 DOWNT0 0)
FDLUTCS_H      : std_logic_vector(1 DOWNT0 0)
GCLK0S         : std_ulogic
IRQ_X          : std_logic
JUNK_UNUSED    : std_logic
LUM            : std_logic_vector(3 DOWNT0 0)
MON_F3124      : std_logic_vector(31 DOWNT0 0)
NDTACK_TCS     : std_logic
NEN_BUSSW      : std_logic
NEN_EVMLINK    : std_logic
NEN_FASTSIGS   : std_logic
NEN_OUT_DAQ    : std_logic
NEN_OUT_PART   : std_logic
NL1A_TCS_LED   : std_logic
NL1A_TCS_MON   : std_logic
NSTATUS_LED    : std_logic_vector(2 DOWNT0 0)
OUT_DAQ0       : std_logic_vector(3 DOWNT0 0)
OUT_DAQ1       : std_logic_vector(3 DOWNT0 0)
OUT_DAQ2       : std_logic_vector(3 DOWNT0 0)
OUT_DAQ3       : std_logic_vector(3 DOWNT0 0)
OUT_DAQ4       : std_logic_vector(3 DOWNT0 0)
OUT_DAQ5       : std_logic_vector(3 DOWNT0 0)
OUT_DAQ6       : std_logic_vector(3 DOWNT0 0)
OUT_DAQ7       : std_logic_vector(3 DOWNT0 0)
OUT_PART24     : std_logic_vector(3 DOWNT0 1)
OUT_PART25     : std_logic_vector(3 DOWNT0 1)
OUT_PART26     : std_logic_vector(3 DOWNT0 1)
OUT_PART27     : std_logic_vector(3 DOWNT0 1)
OUT_PART28     : std_logic_vector(3 DOWNT0 1)
OUT_PART29     : std_logic_vector(3 DOWNT0 1)
OUT_PART30     : std_logic_vector(3 DOWNT0 1)
OUT_PART31     : std_logic_vector(3 DOWNT0 1)
STOP_MON       : std_logic
TEST1_TCS     : std_logic

```

Package List

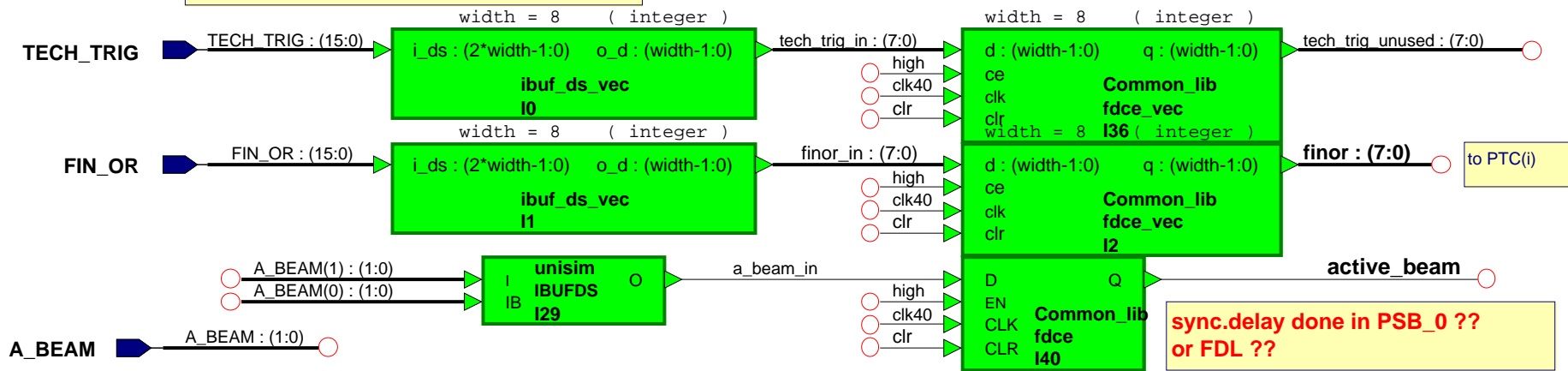
```

LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
USE ieee.STD_LOGIC_UNSIGNED.all;
LIBRARY unisim;
USE unisim.VCOMPONENTS.all;
USE IEEE.VITAL_Timing.all;
LIBRARY STD;
USE STD.TEXTIO.all;
USE unisim.VPKG.all;
LIBRARY tcs_types;
USE tcs_types.tcs.all;
USE IEEE.VITAL_Primitives.all;

```

Vienna		Project:	tcs_chip
		<enter comments here>	
Title:	TCS CHIP		
Path:	tcs_chip_lib/tcs_chip/struct		
Edited:	by taurok on 15 Jän 2008		

I/O FDL board



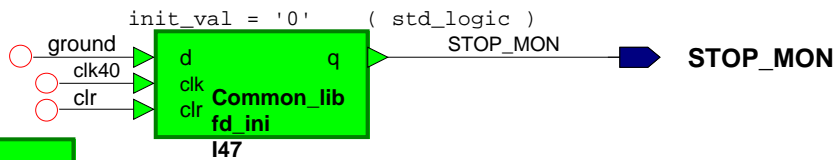
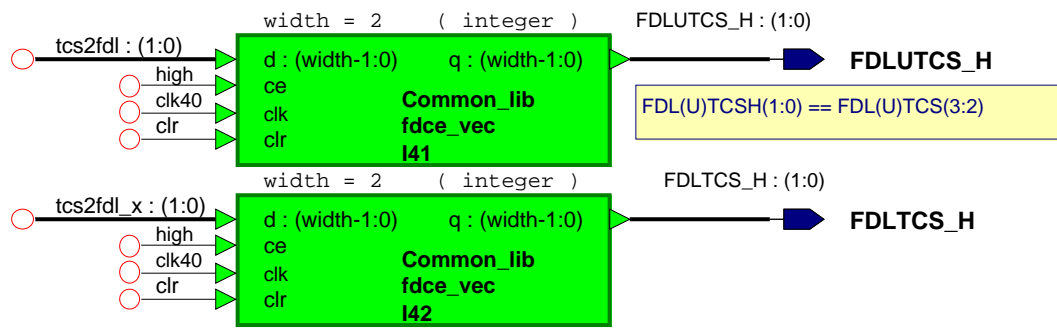
```

eb2
2
-- eb2 2
tcs2fdl(1) <= '0'; ---freeze ???!
tcs2fdl(0) <= new_lum_seg; -- res_fdlcntrs;
tcs2fdl_x(1) <= '0'; ---freeze ???!
tcs2fdl_x(0) <= new_lum_seg; -- res_fdlcntrs;
    
```

FDL(U)TCS:TCS --> FDL (3:2): 3 FREEZE_MON, 2 new_lum_seg
 FDL(U)TCS: TCS <-- FDL (1:0): "00" ... not used

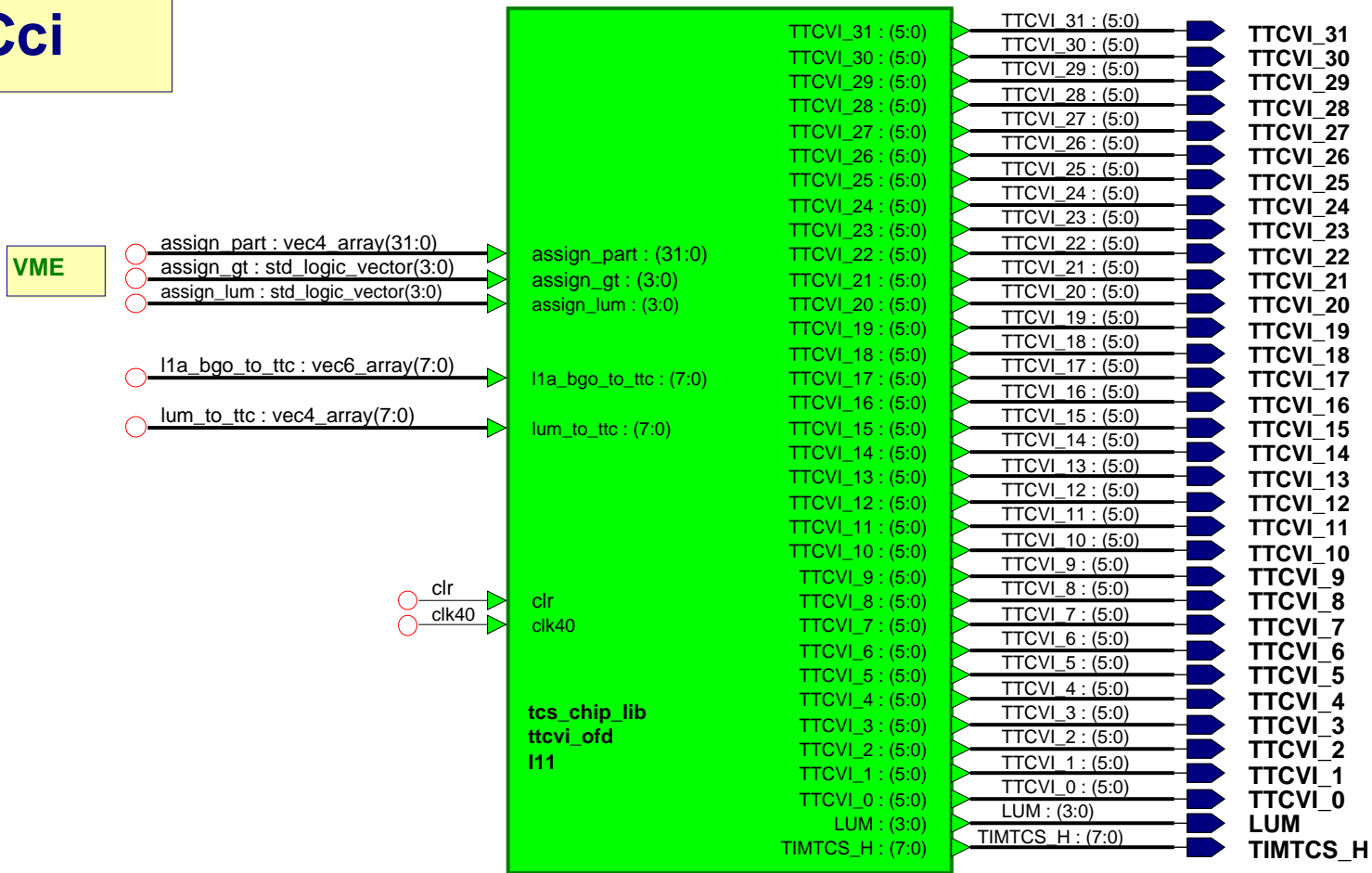
TCS -->TIM (15:8): 15 L1A_FROM_TCS,
 12-8 TCS_BGO(4:0)

TCS <--TIM (7:0): 7 - 4 dummy L1_RES (TIM_V1003)
 3 - 0 TIM_FASTSIG(3:0) (TIM_V1003)



Keep unused Inputs

OUTPUT to TTCci



```

-- V0016: reset orbit counter by PTC0 : bgo_ctrl, tim_signal_decoder modified, requestFF
--       TCS-->FDL: new_lum_seg --> FDLTCSH(0) and FDLUTCSH(0)
--       freeze ....not implemented
--       PTC_SM: resync0 --> init...and continue run
--       ROP: include 'tcs2daq' (=ptc_status) into record
--       'rndm_prescale_fact'....prescaler for random trigger
-- V0015: ... TO BE USED in GLOBAL RUN Nov.2007
--       BAD CODE problem is postponed to a later version.
--       PTC_SM:
--       Starts independently from input status.
--       PANIC BUTTON returns ptc_sm to IDLE status if 'done' bit is missing
--       because the BC-table does not contain the bit for this BGo command.
--       ptc_clears_orbitnr = '1' ..optional reset of orbit counter
--       IDLE:stop_run_fsm_cld <= '1' ; ' =ignore old stop request
--       'hard_res' is possible when in out_of_sync status

V0014: testmask0-7 bits added, ... TO BE USED in GLOBAL RUN Nov.2007
V0013: trigger, bgo_ctrl, vme_decoder_tcs, vme registers_tcs: 'not' set between (...)
       vme_decoder_tcs: dtck_wff delayed by 1 tick
       ptc_sm: After Hardres do a Resync procedure
V0012: bgo_ctrl: removed FF for Emu signals to add OUTFF in 'fast_sig_out' module'
       PTC_SM : resync from error possible, inc_res_cntr inserted
       States out_of_sync+error: -- sensible to 'disconnected' input.
-- can return to busy when err/outsync disappear
V0011: PTC_SM : resync and hardres is possible from warn,ready,busy states
V0010: Evnr+TrigNr start with =1 as in GTFE, board_id =cc07
       Display unit
V000F: pipeline instead of roc state machine sends event records to GTFE
V000E: rop without CASE..--> same as V000D
V000D: test_mask8 bits, nen_evmlink
V000C: PTC-SM with resync,hardres; test_mask bits,
       EMU output corrected
       +/-2bx deadtime around Bgo commands
       new deadtime counter: +/-2bx around BC0; StartofGap
V000B: Monitoring counters,
       PTC-SM without automatic resync; fsm_states register
V000A: fast_sig_decoder
V0009: fast_sig_decod, dtack for ptc_cmd_puls
V0008: first version,

```

```

TEST2_TCS          : std_logic
TIMTCS_H           : std_logic_vector(7 DOWNTO 0)
TTCVI_0            : std_logic_vector(5 DOWNTO 0)
TTCVI_1            : std_logic_vector(5 DOWNTO 0)
TTCVI_10           : std_logic_vector(5 DOWNTO 0)
TTCVI_11           : std_logic_vector(5 DOWNTO 0)
TTCVI_12           : std_logic_vector(5 DOWNTO 0)
TTCVI_13           : std_logic_vector(5 DOWNTO 0)
TTCVI_14           : std_logic_vector(5 DOWNTO 0)
TTCVI_15           : std_logic_vector(5 DOWNTO 0)
TTCVI_16           : std_logic_vector(5 DOWNTO 0)
TTCVI_17           : std_logic_vector(5 DOWNTO 0)
TTCVI_18           : std_logic_vector(5 DOWNTO 0)
TTCVI_19           : std_logic_vector(5 DOWNTO 0)
TTCVI_2            : std_logic_vector(5 DOWNTO 0)
TTCVI_20           : std_logic_vector(5 DOWNTO 0)
TTCVI_21           : std_logic_vector(5 DOWNTO 0)
TTCVI_22           : std_logic_vector(5 DOWNTO 0)
TTCVI_23           : std_logic_vector(5 DOWNTO 0)
TTCVI_24           : std_logic_vector(5 DOWNTO 0)
TTCVI_25           : std_logic_vector(5 DOWNTO 0)
TTCVI_26           : std_logic_vector(5 DOWNTO 0)
TTCVI_27           : std_logic_vector(5 DOWNTO 0)
TTCVI_28           : std_logic_vector(5 DOWNTO 0)
TTCVI_29           : std_logic_vector(5 DOWNTO 0)
TTCVI_3            : std_logic_vector(5 DOWNTO 0)
TTCVI_30           : std_logic_vector(5 DOWNTO 0)
TTCVI_31           : std_logic_vector(5 DOWNTO 0)
TTCVI_4            : std_logic_vector(5 DOWNTO 0)
TTCVI_5            : std_logic_vector(5 DOWNTO 0)
TTCVI_6            : std_logic_vector(5 DOWNTO 0)
TTCVI_7            : std_logic_vector(5 DOWNTO 0)
TTCVI_8            : std_logic_vector(5 DOWNTO 0)
TTCVI_9            : std_logic_vector(5 DOWNTO 0)
VD_I               : std_logic_vector(15 DOWNTO 0)

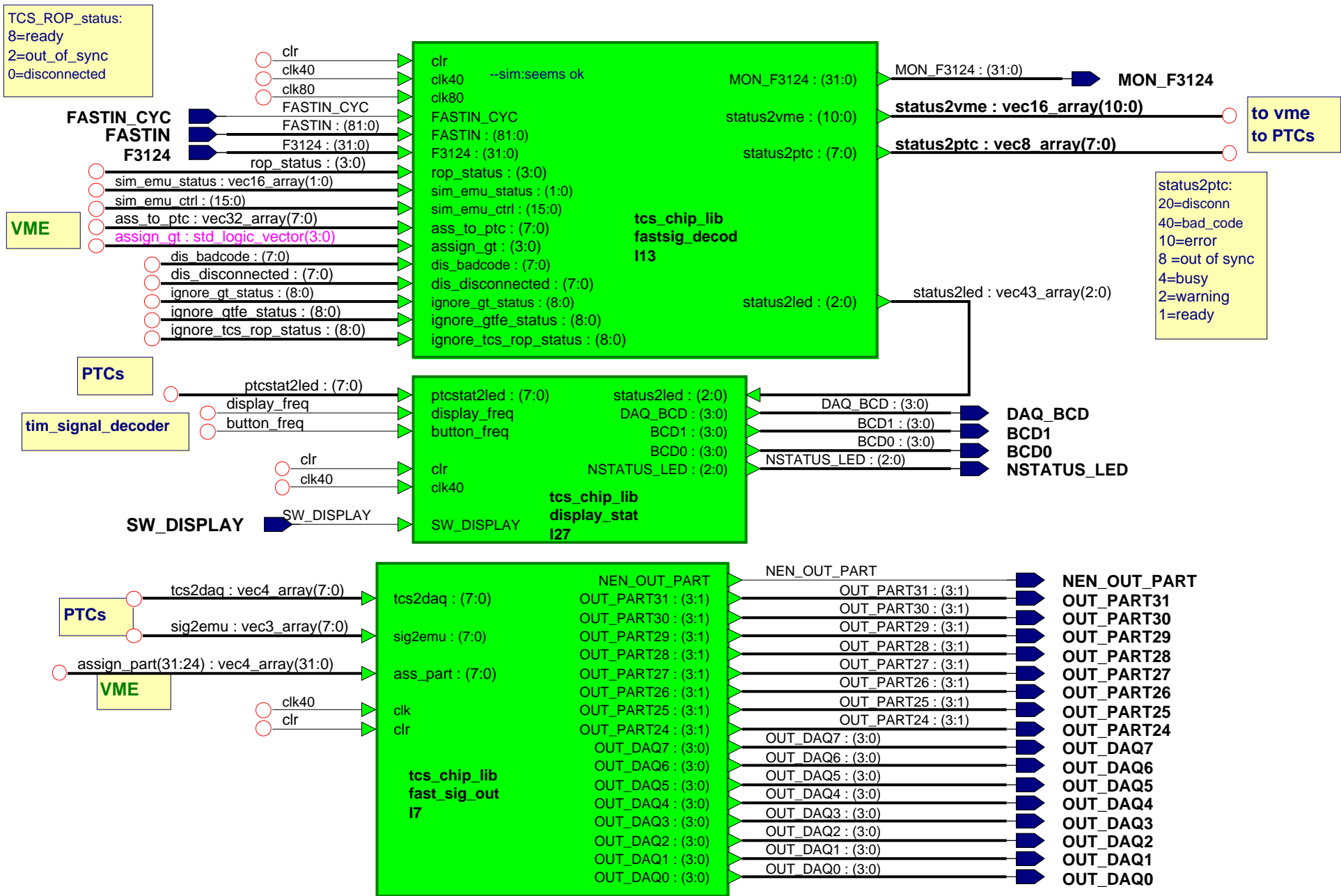
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Diagram Signals:

```

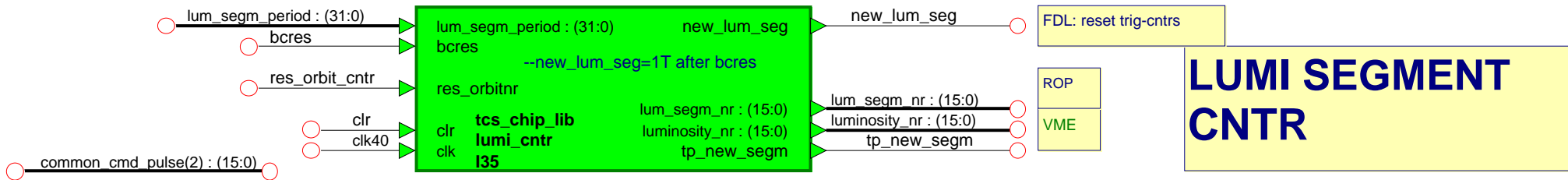
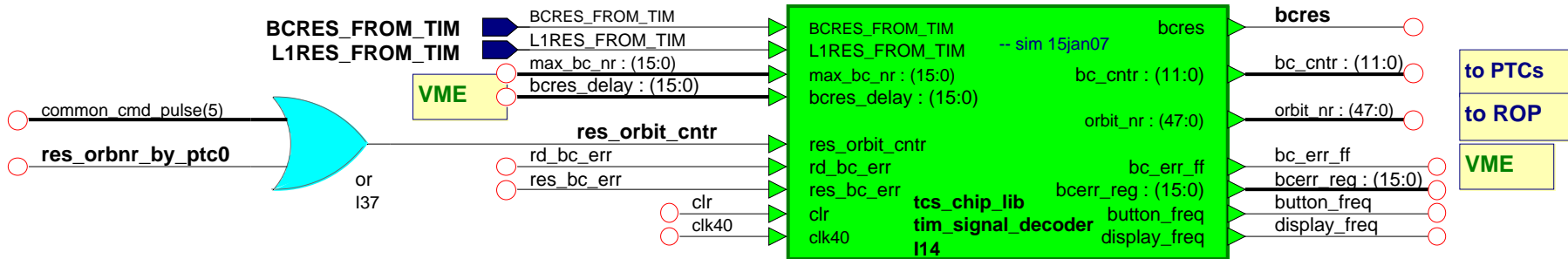
SIGNAL CLK0        : std_ulogic := '0'
SIGNAL CLK180      : std_ulogic := '0'
SIGNAL CLK2X       : std_ulogic := '0'
SIGNAL CLK2X180    : std_ulogic := '0'
SIGNAL CLKIN       : std_logic
SIGNAL a_beam_in   : std_logic
SIGNAL active_beam : std_logic
SIGNAL ass_to_ptc  : vec32_array(7 DOWNTO 0)
SIGNAL assign_gt   : std_logic_vector(3 DOWNTO 0)
SIGNAL assign_lum  : std_logic_vector(3 DOWNTO 0)
SIGNAL assign_part : vec4_array(31 DOWNTO 0)
SIGNAL bc_cntr     : std_logic_vector(11 downto 0)
SIGNAL bc_err_ff   : std_logic
SIGNAL bcerr_reg   : std_logic_vector(15 DOWNTO 0)
SIGNAL bcrest      : std_logic
SIGNAL bcrest_delay : std_logic_vector(15 DOWNTO 0)
SIGNAL bgo_period_l : vec16_array(7 DOWNTO 0)
SIGNAL bgo_period_s : vec16_array(7 DOWNTO 0)
SIGNAL board_id    : std_logic_vector(15 DOWNTO 0)
SIGNAL board_nr_unused : std_logic_vector(2 DOWNTO 0)
SIGNAL button_freq : std_logic
SIGNAL clk40       : std_logic
SIGNAL clk80       : std_logic
SIGNAL clkfb_unused : STD_ULOGIC
SIGNAL clr         : std_logic
SIGNAL common_cmd_pulse : std_logic_vector(15 DOWNTO 0)
SIGNAL common_status : std_logic_vector(15 DOWNTO 0)
SIGNAL dcm_locked  : std_logic
SIGNAL dis_badcode : std_logic_vector(7 DOWNTO 0)
SIGNAL dis_disconnected : std_logic_vector(7 DOWNTO 0)

```



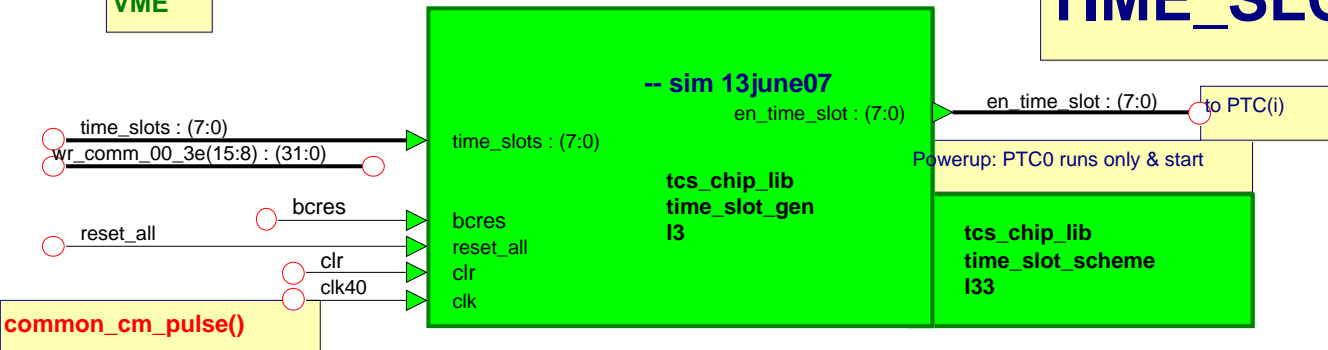
IN/OUT to DET_PART'S, EMULATORS, DAQ_PART'S

BC, ORBIT CNTR



MEMORY XC2V3000: 96 RAMB
8 PTC: bctable=4kx16=4ramb x2 x8 => 64 ramb
Throttle: 16kx1 ==> 1ramb
Timeslot: ==> 1 ramb
ROP: depends from words 5.6 ramb
Sum = 72

TIME_SLOT & THROTTLE



PTC1_7: FOR i IN 1 TO 7 GENERATE



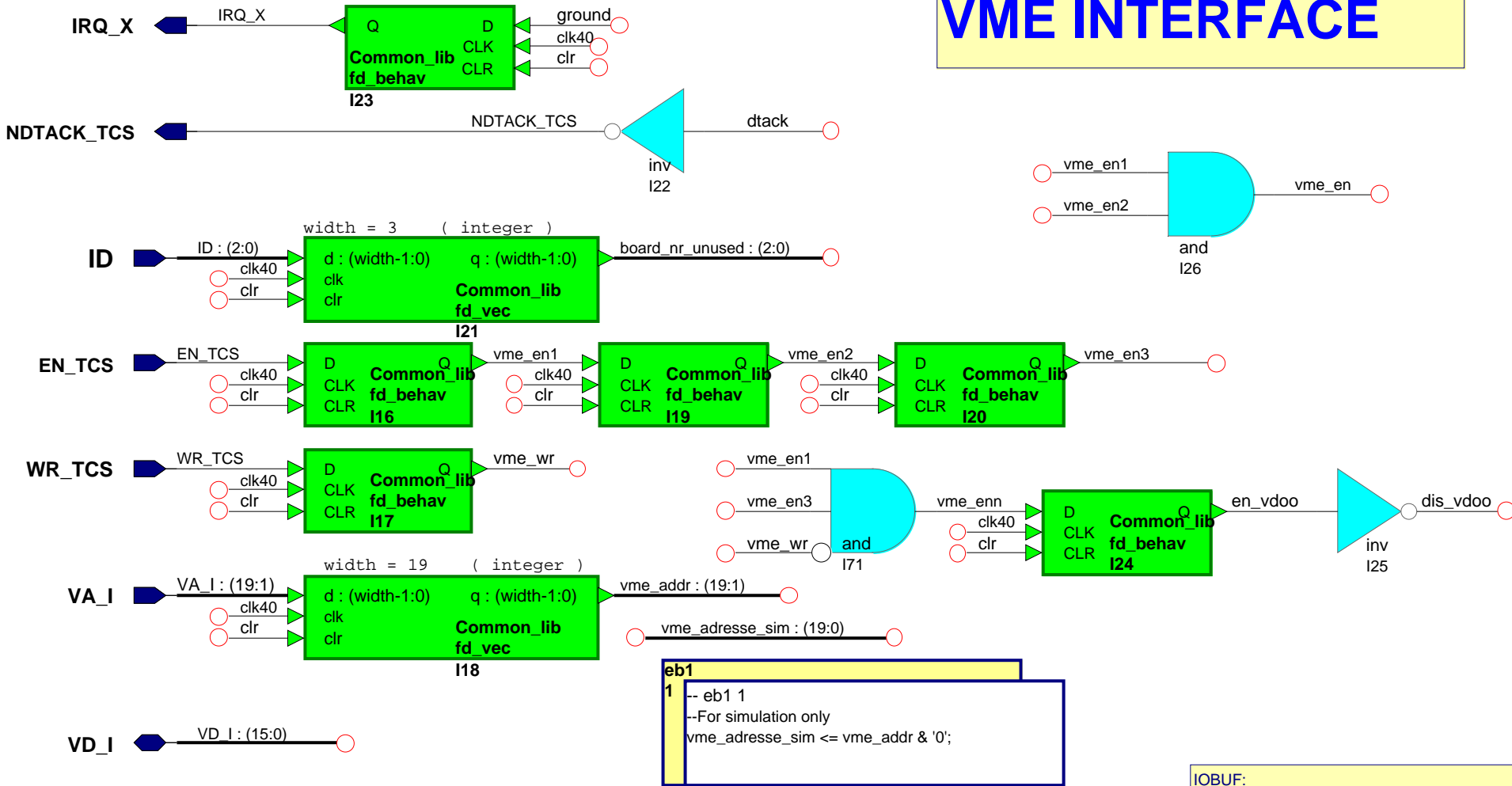
Frame Declarations

```

SIGNAL ais_vdoo          : std_logic
SIGNAL disable_io       : std_logic_vector(3 DOWNTO 0)
SIGNAL display_freq     : std_logic
SIGNAL dout             : std_logic
SIGNAL dtack            : std_logic
SIGNAL en_bctable       : vec2_array(7 DOWNTO 0)
SIGNAL en_time_slot     : std_logic_vector(7 DOWNTO 0)
SIGNAL en_vdoo          : std_logic
SIGNAL event_nr         : vec32_array(7 DOWNTO 0)
SIGNAL event_type_rop   : vec4_array(7 DOWNTO 0)
SIGNAL finor            : std_logic_vector(7 DOWNTO 0)
SIGNAL finor_in         : std_logic_vector(7 DOWNTO 0)
SIGNAL ground           : std_logic
SIGNAL gsr              : STD_ULOGIC
SIGNAL gts              : std_ulogic
SIGNAL high             : std_logic
SIGNAL ignore_gt_status : std_logic_vector(8 DOWNTO 0)
SIGNAL ignore_gtfe_status : std_logic_vector(8 DOWNTO 0)
SIGNAL ignore_tcs_rop_status : std_logic_vector(8 DOWNTO 0)
SIGNAL incr_deadt_cntr  : vec11_array(7 DOWNTO 0)
SIGNAL incr_trig_cntr   : vec8_array(7 DOWNTO 0)
SIGNAL inh_low_rate     : std_logic
SIGNAL inh_norm_rate    : std_logic
SIGNAL l1a2front        : std_logic_vector(7 DOWNTO 0)
SIGNAL l1a2rop          : std_logic_vector(7 DOWNTO 0)
SIGNAL l1a2throttle     : std_logic_vector(7 DOWNTO 0)
SIGNAL l1a_bgo_to_ttc   : vec6_array(7 DOWNTO 0)
SIGNAL ld_rule4         : std_logic
SIGNAL lum_seg_m_nr     : std_logic_vector(15 DOWNTO 0)
SIGNAL lum_seg_m_period : std_logic_vector(31 DOWNTO 0)
SIGNAL lum_to_ttc       : vec4_array(7 DOWNTO 0)
SIGNAL luminosity_nr    : std_logic_vector(15 DOWNTO 0)
SIGNAL max_bc_nr        : std_logic_vector(15 DOWNTO 0)
SIGNAL nclk40           : std_logic
SIGNAL nclk80           : std_logic
SIGNAL new_lum_seg      : std_logic
SIGNAL orbit_nr         : std_logic_vector(47 DOWNTO 0)
SIGNAL part_run_nr      : vec32_array(7 DOWNTO 0)
SIGNAL ptc0_clears_orbitnr : std_logic
SIGNAL ptc2tp           : vec8_array(7 DOWNTO 0)
SIGNAL ptc2tp0          : std_logic_vector(7 DOWNTO 0)
SIGNAL ptc2tp1          : std_logic_vector(7 DOWNTO 0)
SIGNAL ptc2tp2          : std_logic_vector(7 DOWNTO 0)
SIGNAL ptc2tp3          : std_logic_vector(7 DOWNTO 0)
SIGNAL ptc2tp4          : std_logic_vector(7 DOWNTO 0)
SIGNAL ptc2tp5          : std_logic_vector(7 DOWNTO 0)
SIGNAL ptc2tp6          : std_logic_vector(7 DOWNTO 0)
SIGNAL ptc2tp7          : std_logic_vector(7 DOWNTO 0)
SIGNAL ptc_cmd_pulse    : vec16_array(7 DOWNTO 0)
SIGNAL ptc_cmd_reg      : vec16_array(7 DOWNTO 0)
SIGNAL ptc_emu_delay     : vec16_array(7 DOWNTO 0)
SIGNAL ptc_fsm_states   : vec16_array(7 DOWNTO 0)
SIGNAL ptc_status       : vec16_array(7 DOWNTO 0)
SIGNAL ptcstat2led      : vec3_array(7 DOWNTO 0)
SIGNAL rd_bc_err        : std_logic
SIGNAL rd_comm_3e       : std_logic
SIGNAL rd_comm_40_6e    : std_logic_vector(23 DOWNTO 0)
SIGNAL rd_comm_b0_be    : std_logic_vector(7 DOWNTO 0)
SIGNAL rd_deadt_cntr    : vec32_array(7 DOWNTO 0)
SIGNAL rd_ptci_l0_le    : vec8_array(7 DOWNTO 0)
SIGNAL rd_trig_cntr     : vec16_array(7 DOWNTO 0)
SIGNAL rdbk_comm_reg    : std_logic
SIGNAL rdbk_ptc_reg     : std_logic
SIGNAL recover_time     : std_logic_vector(15 DOWNTO 0)
SIGNAL res_bc_err       : std_logic
SIGNAL res_deadt_cntr   : vec11_array(7 DOWNTO 0)
SIGNAL res_orbit_cntr   : std_logic

```

VME INTERFACE

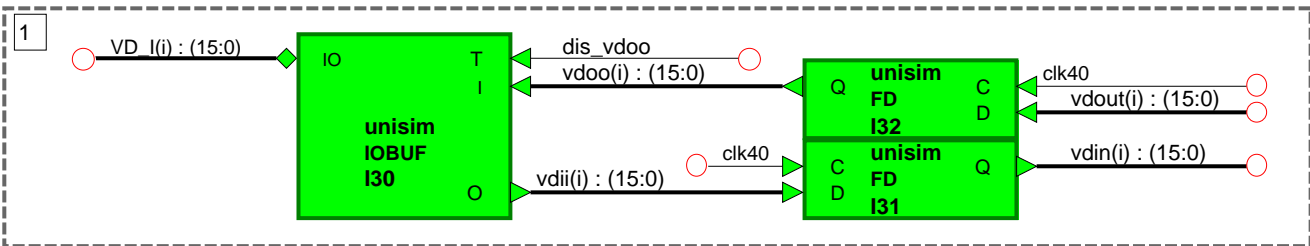


```

eb1
1
-- eb1 1
--For simulation only
vme_adresse_sim <= vme_addr & '0';
    
```

IOBUF:
 T= 1: IO=Z, O=X vme writing or inactive
 T= 0: IO=I, O=I vme read

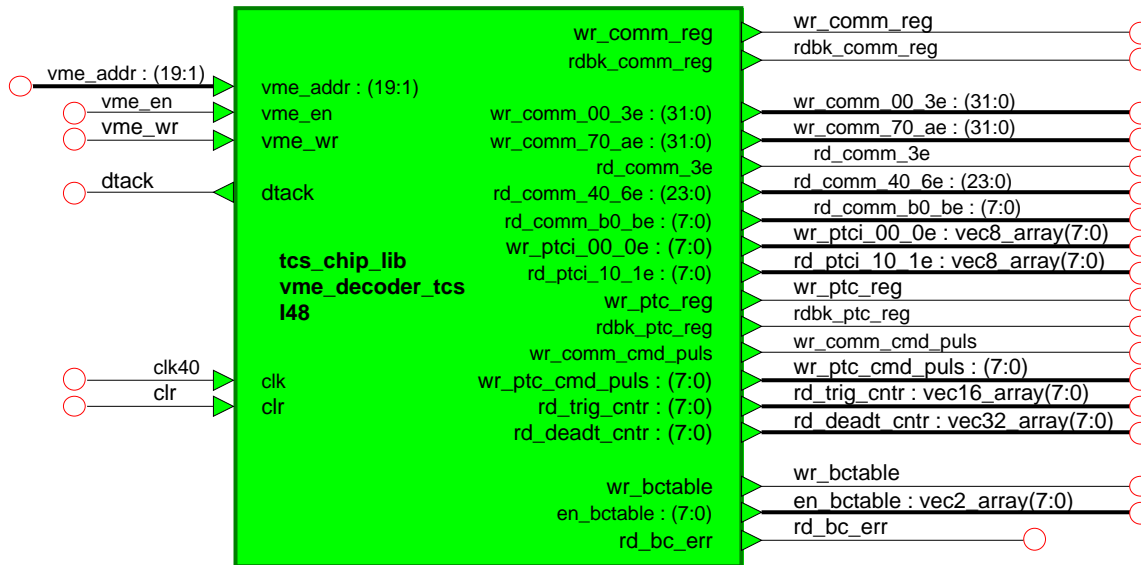
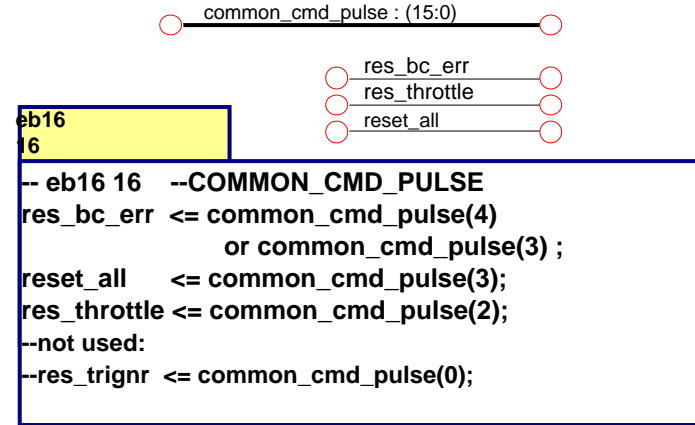
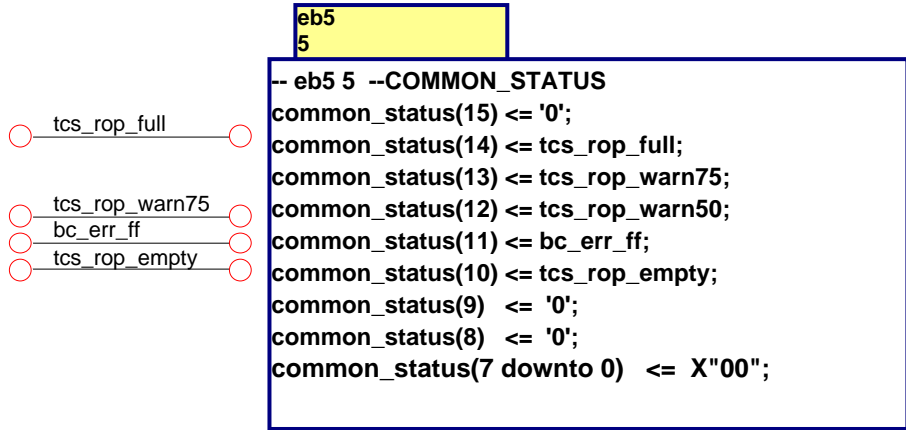
g0: FOR i IN 0 TO 15 GENERATE



BIDIRECTIONAL VME DATA BUS

Frame Declarations

VME registers



PTC_i w/r regs

Common w/r regs

PTC_0



```

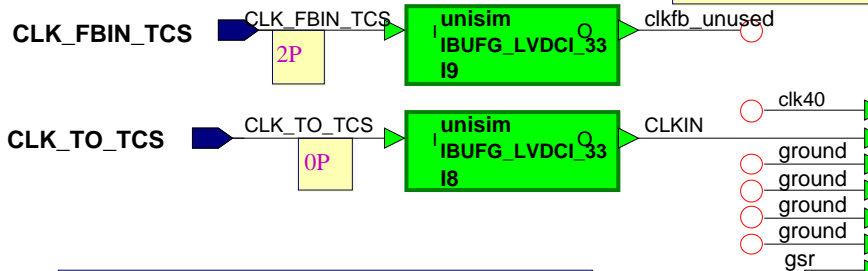
SIGNAL res_orbnr_by_ptc0 : std_logic
SIGNAL res_orbnr_by_ptc0 : std_logic
SIGNAL res_throttle : std_logic
SIGNAL res_trig_cntr : vec8_array(7 DOWNTO 0)
SIGNAL reset_all : std_logic
SIGNAL rndm_period : vec16_array(7 DOWNTO 0)
SIGNAL rndm_prescale_fact : vec16_array(7 DOWNTO 0)
SIGNAL rop_status : std_logic_vector(3 DOWNTO 0)
SIGNAL settle_time : std_logic_vector(15 DOWNTO 0)
SIGNAL sig2emu : vec3_array(7 DOWNTO 0)
SIGNAL sig2emu_tp0 : std_logic_vector(2 DOWNTO 0)
SIGNAL sig2emu_tp1 : std_logic_vector(2 DOWNTO 0)
SIGNAL sig2emu_tp2 : std_logic_vector(2 DOWNTO 0)
SIGNAL sig2emu_tp3 : std_logic_vector(2 DOWNTO 0)
SIGNAL sig2emu_tp4 : std_logic_vector(2 DOWNTO 0)
SIGNAL sig2emu_tp5 : std_logic_vector(2 DOWNTO 0)
SIGNAL sig2emu_tp6 : std_logic_vector(2 DOWNTO 0)
SIGNAL sig2emu_tp7 : std_logic_vector(2 DOWNTO 0)
SIGNAL sim_emu_ctrl : std_logic_vector(15 DOWNTO 0)
SIGNAL sim_emu_status : vec16_array(1 DOWNTO 0)
SIGNAL status2led : vec43_array(2 DOWNTO 0)
SIGNAL status2ptc : vec8_array(7 DOWNTO 0)
SIGNAL status2vme : vec16_array(10 DOWNTO 0)
SIGNAL switch_tp2pan : std_logic_vector(15 DOWNTO 0)
SIGNAL tcs2daq : vec4_array(7 DOWNTO 0)
SIGNAL tcs2fdl : std_logic_vector(1 DOWNTO 0)
SIGNAL tcs2fdl_x : std_logic_vector(1 DOWNTO 0)
SIGNAL tcs_rop_empty : std_logic
SIGNAL tcs_rop_full : std_logic
SIGNAL tcs_rop_warn50 : std_logic
SIGNAL tcs_rop_warn75 : std_logic
SIGNAL tech_trig_in : std_logic_vector(7 DOWNTO 0)
SIGNAL tech_trig_unused : std_logic_vector(7 DOWNTO 0)
SIGNAL test_sig0 : std_logic_vector(15 DOWNTO 0)
SIGNAL test_sig1 : std_logic_vector(15 DOWNTO 0)
SIGNAL test_sig2 : std_logic_vector(15 DOWNTO 0)
SIGNAL test_sig3 : std_logic_vector(15 DOWNTO 0)
SIGNAL test_sig4 : std_logic_vector(15 DOWNTO 0)
SIGNAL test_sig5 : std_logic_vector(15 DOWNTO 0)
SIGNAL test_sig6 : std_logic_vector(15 DOWNTO 0)
SIGNAL test_sig7 : std_logic_vector(15 DOWNTO 0)
SIGNAL test_sig8 : std_logic_vector(15 DOWNTO 0)
SIGNAL test_signal : vec16_array(8 DOWNTO 0)
SIGNAL testmasks : vec16_array(8 DOWNTO 0)
SIGNAL thr_rule : std_logic_vector(127 DOWNTO 0)
SIGNAL time_slots : vec16_array(7 DOWNTO 0)
SIGNAL tp_eor : std_logic
SIGNAL tp_header : std_logic_vector(3 DOWNTO 0)
SIGNAL tp_new_segm : std_logic
SIGNAL tp_sel_word0 : std_logic
SIGNAL tp_thro_inh : std_logic_vector(7 DOWNTO 0)
SIGNAL trig_nr : vec32_array(7 DOWNTO 0)
SIGNAL trig_type_a : vec16_array(7 DOWNTO 0)
SIGNAL trig_type_b : vec16_array(7 DOWNTO 0)
SIGNAL v_bc_table0 : vec16_array(7 DOWNTO 0)
SIGNAL v_bc_table1 : vec16_array(7 DOWNTO 0)
SIGNAL v_cntrs : vec16_array(7 DOWNTO 0)
SIGNAL vdii : std_logic_vector(15 DOWNTO 0)
SIGNAL vdin : std_logic_vector(15 DOWNTO 0)
SIGNAL vdoo : std_logic_vector(15 DOWNTO 0)
SIGNAL vdout : std_logic_vector(15 DOWNTO 0)
SIGNAL vme_addr : std_logic_vector(19 DOWNTO 1)
SIGNAL vme_adresse_sim : std_logic_vector(19 DOWNTO 0)
SIGNAL vme_en : std_logic
SIGNAL vme_en1 : std_logic
SIGNAL vme_en2 : std_logic
SIGNAL vme_en3 : std_logic

```

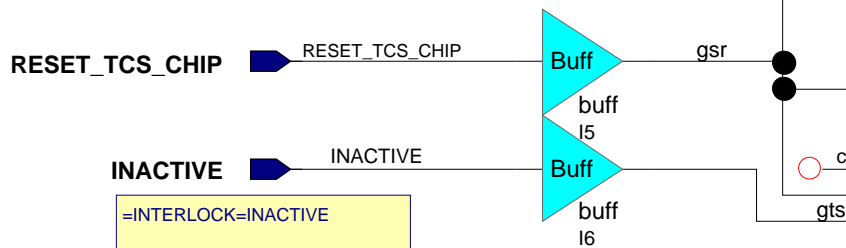
DCM & CLOCK

We could also take clock_dcm from psb_lib or clock_module from common_lib.

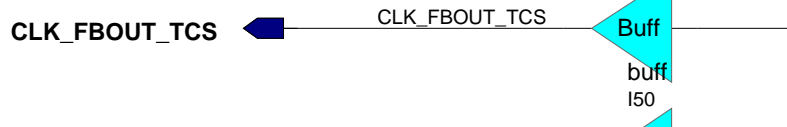
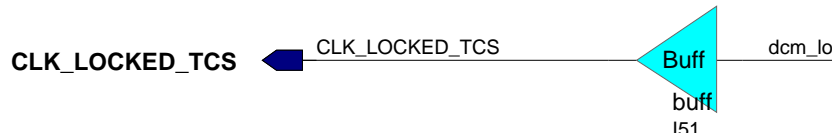
CLKFB not used, maybe later.
==> to unused



IBUFG and IBUF are placed on uppermost hierarchy.

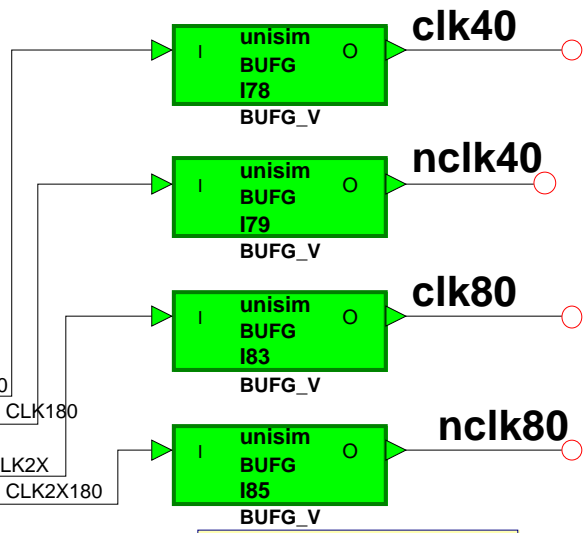
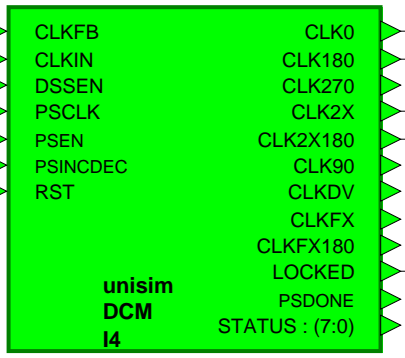


=INTERLOCK=INACTIVE

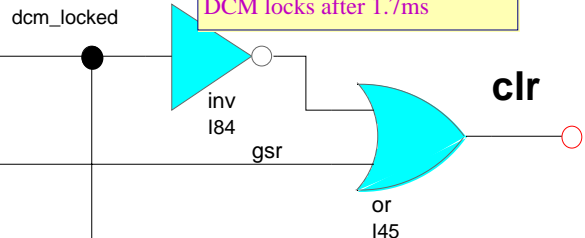


TP on MEZZ board

GTS=1 ==> All IOB into highZ
GSR=1 ==> Reset/Set set all FF



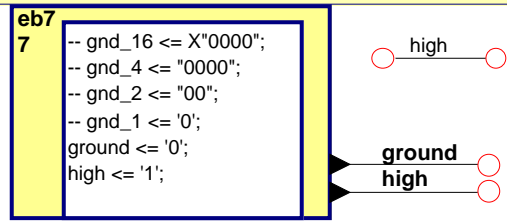
Simulation ok.
DCM locks after 1.7ms



TCS: CLEAR all by VME chip

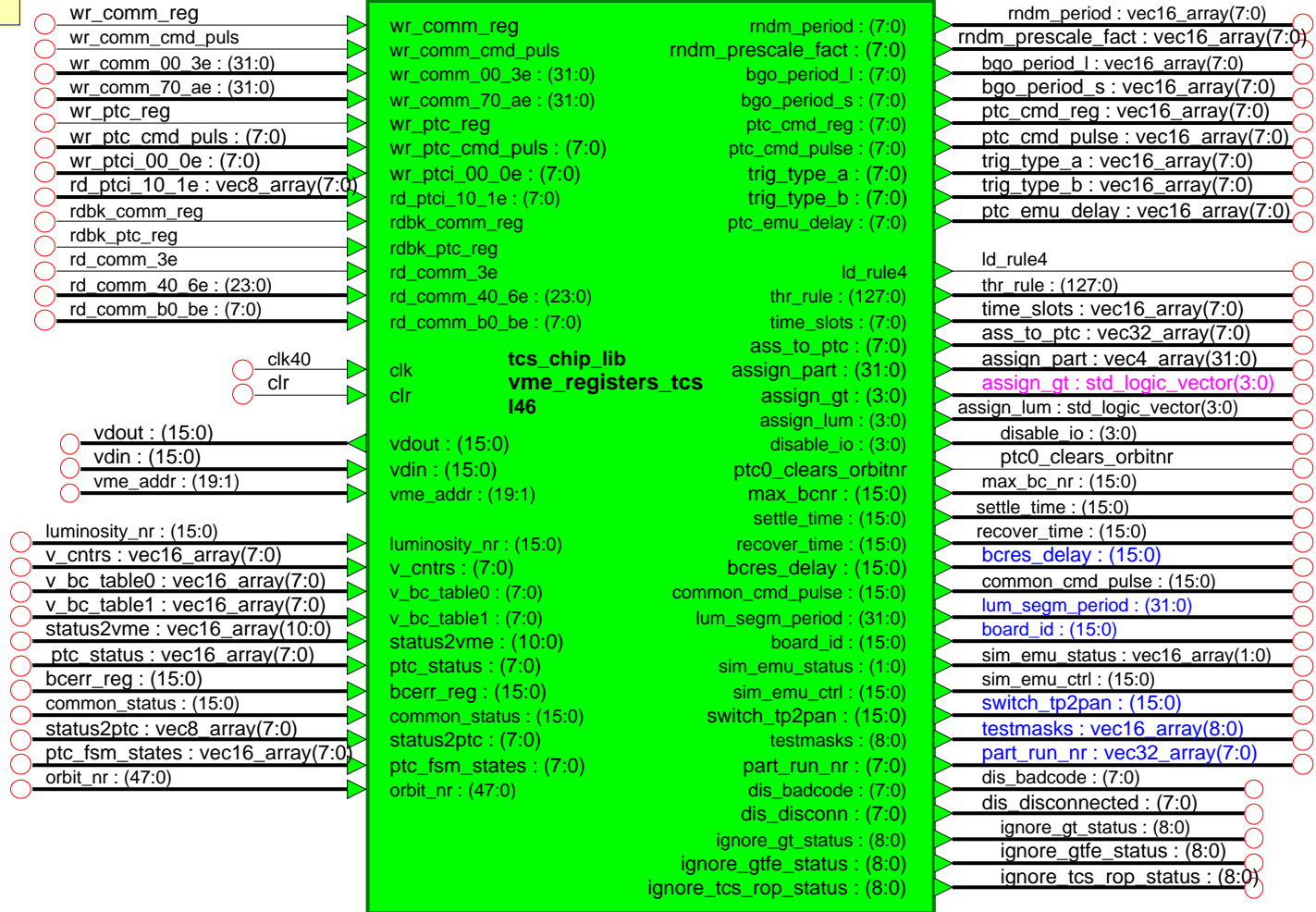
FDL, PSB, TIM
clr <= not clk_locked

For Synthesis add --pragma synthesis_off/on around generics
rightMouse==> select Object Properties==>Generics
and activate 'add pragmas around generics'



VME registers

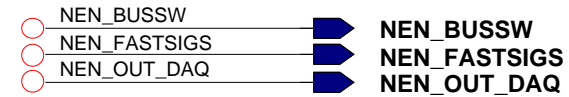
```
version_nr_h = X"0000" ( std_logic_vector(15 downto 0) )
version_nr_l = X"0016" ( std_logic_vector(15 downto 0) )
```



```
eb18 -- eb18 18
18 NEN_BUSSW <= disable_io(3);
-- automatic generation in tcs_rop;
-- NEN_EVM_LINK <= disable_io(2);
NEN_FASTSIGS <= disable_io(1);
NEN_OUT_DAQ <= disable_io(0);
```

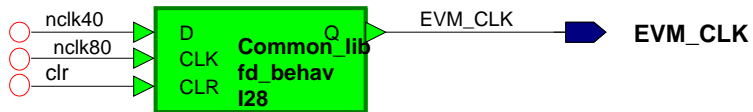
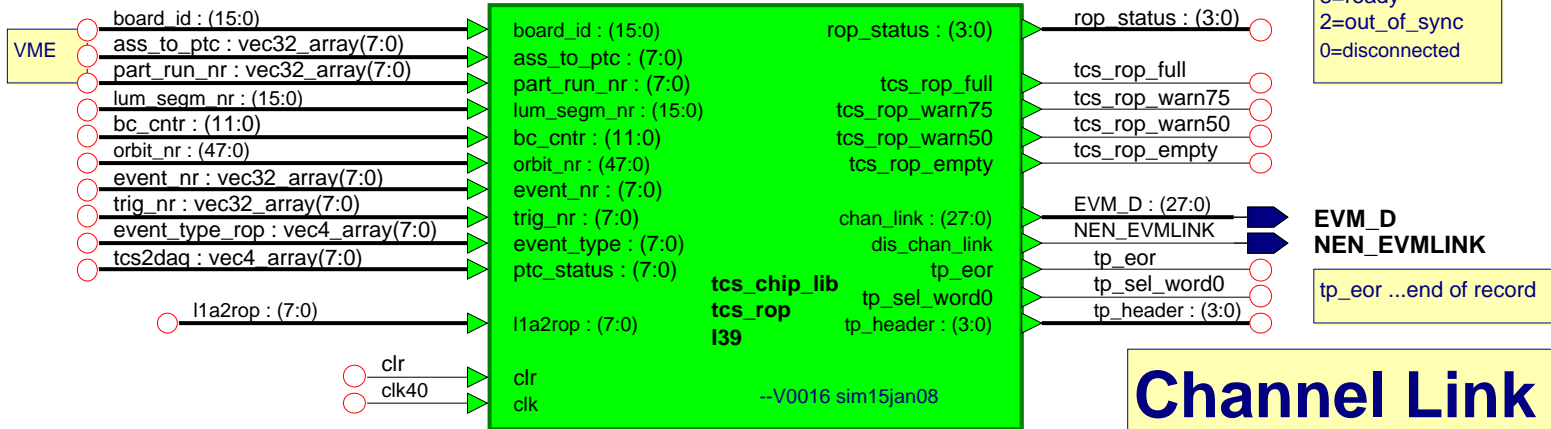
RATE COUNTERS: 32 bits (12h/100kHz) --> 2 words
 DEADTIME COUNTERS: 40 bits(7h/40MHz) -->48 --> 3 words+1free

w/r regs: load all into a RAM and read them back from it.



ROP

If L1A arrives then send a record.



EVM_CLK = clk40 delayed by 6.2 ns to write safely into then Channel Link chip.

tp_thro_inh(0) : (7:0)

```
SIGNAL vme_enn      : std_logic
SIGNAL vme_wr       : std_logic
SIGNAL wr_bctable   : std_logic
SIGNAL wr_comm_00_3e : std_logic_vector(31 DOWNTO 0)
SIGNAL wr_comm_70_ae : std_logic_vector(31 DOWNTO 0)
SIGNAL wr_comm_cmd_puls : std_logic
SIGNAL wr_comm_reg  : std_logic
SIGNAL wr_ptc_cmd_puls : std_logic_vector(7 DOWNTO 0)
SIGNAL wr_ptc_reg    : std_logic
SIGNAL wr_ptci_00_0e : vec8_array(7 downto 0)
```

```

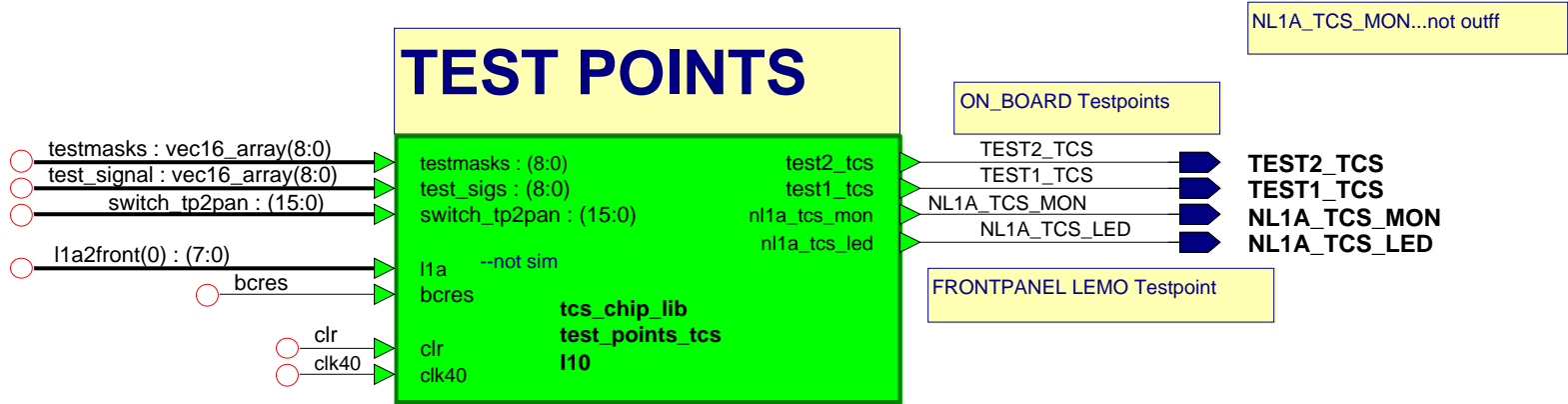
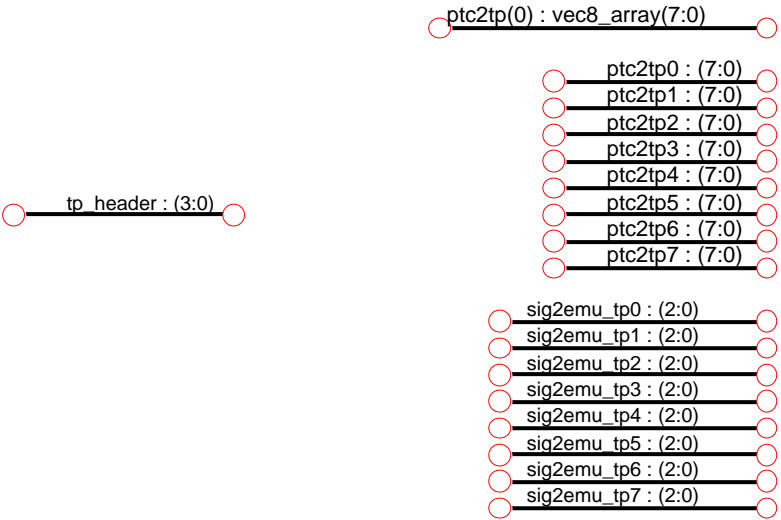
TimingChecksOn          = true                ( boolean )
InstancePath            = "*"                ( string )
Xon                     = true                ( boolean )
MsgOn                   = false               ( boolean )
thold_PSEN_PSCLK_negedge_posedge = 0.000 ns ( VitalDelayType )
thold_PSEN_PSCLK_posedge_posedge = 0.000 ns ( VitalDelayType )
thold_PSINCDEC_PSCLK_negedge_posedge = 0.000 ns ( VitalDelayType )
thold_PSINCDEC_PSCLK_posedge_posedge = 0.000 ns ( VitalDelayType )
tipd_CLKFB              = (0.000 ns, 0.000 ns) ( VitalDelayType01 )
tipd_CLKIN              = (0.000 ns, 0.000 ns) ( VitalDelayType01 )
tipd_DSSEN              = (0.000 ns, 0.000 ns) ( VitalDelayType01 )
tipd_PSCLK              = (0.000 ns, 0.000 ns) ( VitalDelayType01 )
tipd_PSEN               = (0.000 ns, 0.000 ns) ( VitalDelayType01 )
tipd_PSINCDEC           = (0.000 ns, 0.000 ns) ( VitalDelayType01 )
tipd_RST                = (0.000 ns, 0.000 ns) ( VitalDelayType01 )
tpd_CLKIN_LOCKED        = (0.000 ns, 0.000 ns) ( VitalDelayType01 )
tpd_PSCLK_PSDONE        = (0.000 ns, 0.000 ns) ( VitalDelayType01 )
tperiod_CLKIN_POSEDGE   = 0.000 ns           ( VitalDelayType )
tperiod_PSCLK_POSEDGE   = 0.000 ns           ( VitalDelayType )
tpw_CLKIN_negedge       = 0.000 ns           ( VitalDelayType )
tpw_CLKIN_posedge       = 0.000 ns           ( VitalDelayType )
tpw_PSCLK_negedge       = 0.000 ns           ( VitalDelayType )
tpw_PSCLK_posedge       = 0.000 ns           ( VitalDelayType )
tpw_RST_posedge         = 0.000 ns           ( VitalDelayType )
tsetup_PSEN_PSCLK_negedge_posedge = 0.000 ns ( VitalDelayType )
tsetup_PSEN_PSCLK_posedge_posedge = 0.000 ns ( VitalDelayType )
tsetup_PSINCDEC_PSCLK_negedge_posedge = 0.000 ns ( VitalDelayType )
tsetup_PSINCDEC_PSCLK_posedge_posedge = 0.000 ns ( VitalDelayType )
CLKDV_DIVIDE            = 2.0                ( real )
CLKFX_DIVIDE            = 1                  ( integer )
CLKFX_MULTIPLY          = 4                  ( integer )
CLKIN_DIVIDE_BY_2       = false              ( boolean )
CLKIN_PERIOD            = 0.0                ( real )
CLKOUT_PHASE_SHIFT      = "NONE"             ( string )
CLK_FEEDBACK            = "1X"               ( string )
DESKEW_ADJUST           = "SYSTEM_SYNCHRONOUS" ( string )
DFS_FREQUENCY_MODE      = "LOW"              ( string )
DLL_FREQUENCY_MODE      = "LOW"              ( string )
DSS_MODE                = "NONE"             ( string )
DUTY_CYCLE_CORRECTION   = true              ( boolean )
FACTORY_JF               = X"C080"           ( bit_vector )
MAXPERCLKIN             = 1000000 ps         ( time )
MAXPERPSCLK             = 100000000 ps       ( time )
PHASE_SHIFT             = 0                  ( integer )
SIM_CLKIN_CYCLE_JITTER  = 300 ps            ( time )
SIM_CLKIN_PERIOD_JITTER = 1000 ps           ( time )
STARTUP_WAIT            = false              ( boolean )

```

COMMON TEST POINTS

```

eb13
13
--COMMON TESTPOINTS
-- DEFINE test_signal(8)
test_signal(8) <= test_sig8;
test_sig8(15) <= bcrest;
test_sig8(14) <= tcs_rop_full;
test_sig8(13) <= tcs_rop_warn50;
test_sig8(12) <= tcs_rop_empty; --extended length=1 orbit
test_sig8(11) <= tp_new_seg;
test_sig8(10) <= inh_norm_rate;
test_sig8(9) <= inh_low_rate;
test_sig8(8) <= tp_header(3); -- = evm_d(27)
test_sig8(7) <= tp_header(2);
test_sig8(6) <= tp_header(1);
test_sig8(5) <= tp_header(0); -- = evm_d(24)
test_sig8(4) <= vme_en;
test_sig8(3) <= dtack;
test_sig8(2) <= active_beam;
test_sig8(1) <= tp_sel_word0; -- <-- rop: sel_word(0)
test_sig8(0) <= tp_eor; -- <-- rop: end of record
    
```



PTCi TEST POINTS

test sig0 : (15:0)

```

eb3 -- PTC 0 testpoints
3 -- DEFINE test_signal(0)
test_signal(0) <= test_sig0;
sig2emu_tp0 <= sig2emu(0);
ptc2tp0 <= ptc2tp(0);
test_sig0(15) <= l1a2front(0);
test_sig0(14) <= en_time_slot(0);
test_sig0(13) <= '0';
test_sig0(12) <= sig2emu_tp0(2); --bcr
test_sig0(11) <= sig2emu_tp0(1); --resync
test_sig0(10) <= sig2emu_tp0(0); --l1a
test_sig0(9) <= tp_thro_inh(0);
test_sig0(8) <= finor(0); -- from FDL
test_sig0(7) <= ptc2tp0(7); -- low_rate
test_sig0(6) <= ptc2tp0(6); -- norm_rate
test_sig0(5) <= ptc2tp0(5); -- random_trig
test_sig0(4) <= ptc2tp0(4); -- test_trig
test_sig0(3) <= ptc2tp0(3); -- cal_trig
test_sig0(2) <= ptc2tp0(2); -- inh_l1a_test
test_sig0(1) <= ptc2tp0(1); -- inh_l1a_cal
test_sig0(0) <= ptc2tp0(0); -- inh_l1a_priv

```

test sig1 : (15:0)

```

eb4 -- PTC1 testpoints
4 -- DEFINE test_signal(1)
test_signal(1) <= test_sig1;
sig2emu_tp1 <= sig2emu(1);
ptc2tp1 <= ptc2tp(1);
test_sig1(15) <= l1a2front(1);
test_sig1(14) <= en_time_slot(1);
test_sig1(13) <= '0';
test_sig1(12) <= sig2emu_tp1(2);
test_sig1(11) <= sig2emu_tp1(1);
test_sig1(10) <= sig2emu_tp1(0);
test_sig1(9) <= tp_thro_inh(1);
test_sig1(8) <= finor(1);
test_sig1(7) <= ptc2tp1(7);
test_sig1(6) <= ptc2tp1(6);
test_sig1(5) <= ptc2tp1(5);
test_sig1(4) <= ptc2tp1(4);
test_sig1(3) <= ptc2tp1(3);
test_sig1(2) <= ptc2tp1(2);
test_sig1(1) <= ptc2tp1(1);
test_sig1(0) <= ptc2tp1(0);

```

test sig2 : (15:0)

```

eb8 PTC 2 testpoints
8 -- DEFINE test_signal(2)
-- DEFINE test_signal(2)
test_signal(2) <= test_sig2;
sig2emu_tp2 <= sig2emu(2);
ptc2tp2 <= ptc2tp(2);
test_sig2(15) <= l1a2front(2);
test_sig2(14) <= en_time_slot(2);
test_sig2(13) <= '0';
test_sig2(12) <= sig2emu_tp2(2);
test_sig2(11) <= sig2emu_tp2(1);
test_sig2(10) <= sig2emu_tp2(0);
test_sig2(9) <= tp_thro_inh(2);
test_sig2(8) <= finor(2);
test_sig2(7) <= ptc2tp2(7);
test_sig2(6) <= ptc2tp2(6);
test_sig2(5) <= ptc2tp2(5);
test_sig2(4) <= ptc2tp2(4);
test_sig2(3) <= ptc2tp2(3);
test_sig2(2) <= ptc2tp2(2);
test_sig2(1) <= ptc2tp2(1);
test_sig2(0) <= ptc2tp2(0);

```

test sig3 : (15:0)

```

eb9 PTC 3 testpoints
9 -- DEFINE test_signal(3)
-- DEFINE test_signal(3)
test_signal(3) <= test_sig3;
sig2emu_tp3 <= sig2emu(3);
ptc2tp3 <= ptc2tp(3);
test_sig3(15) <= l1a2front(3);
test_sig3(14) <= en_time_slot(3);
test_sig3(13) <= '0';
test_sig3(12) <= sig2emu_tp3(2);
test_sig3(11) <= sig2emu_tp3(1);
test_sig3(10) <= sig2emu_tp3(0);
test_sig3(9) <= tp_thro_inh(3);
test_sig3(8) <= finor(3);
test_sig3(7) <= ptc2tp3(7);
test_sig3(6) <= ptc2tp3(6);
test_sig3(5) <= ptc2tp3(5);
test_sig3(4) <= ptc2tp3(4);
test_sig3(3) <= ptc2tp3(3);
test_sig3(2) <= ptc2tp3(2);
test_sig3(1) <= ptc2tp3(1);
test_sig3(0) <= ptc2tp3(0);

```

test sig4 : (15:0)

```

eb6 -- PTC 4 testpoints
6 -- DEFINE test_signal(4)
test_signal(4) <= test_sig4;
sig2emu_tp4 <= sig2emu(4);
ptc2tp4 <= ptc2tp(4);
test_sig4(15) <= l1a2front(4);
test_sig4(14) <= en_time_slot(4);
test_sig4(13) <= '0';
test_sig4(12) <= sig2emu_tp4(2);
test_sig4(11) <= sig2emu_tp4(1);
test_sig4(10) <= sig2emu_tp4(0);
test_sig4(9) <= tp_thro_inh(4);
test_sig4(8) <= finor(4);
test_sig4(7) <= ptc2tp4(7);
test_sig4(6) <= ptc2tp4(6);
test_sig4(5) <= ptc2tp4(5);
test_sig4(4) <= ptc2tp4(4);
test_sig4(3) <= ptc2tp4(3);
test_sig4(2) <= ptc2tp4(2);
test_sig4(1) <= ptc2tp4(1);
test_sig4(0) <= ptc2tp4(0);

```

test sig5 : (15:0)

```

eb10 -- PTC 5 testpoints
10 -- DEFINE test_signal(5)
test_signal(5) <= test_sig5;
sig2emu_tp5 <= sig2emu(5);
ptc2tp5 <= ptc2tp(5);
test_sig5(15) <= l1a2front(5);
test_sig5(14) <= en_time_slot(5);
test_sig5(13) <= '0';
test_sig5(12) <= sig2emu_tp5(2);
test_sig5(11) <= sig2emu_tp5(1);
test_sig5(10) <= sig2emu_tp5(0);
test_sig5(9) <= tp_thro_inh(5);
test_sig5(8) <= finor(5);
test_sig5(7) <= ptc2tp5(7);
test_sig5(6) <= ptc2tp5(6);
test_sig5(5) <= ptc2tp5(5);
test_sig5(4) <= ptc2tp5(4);
test_sig5(3) <= ptc2tp5(3);
test_sig5(2) <= ptc2tp5(2);
test_sig5(1) <= ptc2tp5(1);
test_sig5(0) <= ptc2tp5(0);

```

test sig6 : (15:0)

```

eb11 -- PTC 6 testpoints
11 -- DEFINE test_signal(6)
test_signal(6) <= test_sig6;
sig2emu_tp6 <= sig2emu(6);
ptc2tp6 <= ptc2tp(6);
test_sig6(15) <= l1a2front(6);
test_sig6(14) <= en_time_slot(6);
test_sig6(13) <= '0';
test_sig6(12) <= sig2emu_tp6(2);
test_sig6(11) <= sig2emu_tp6(1);
test_sig6(10) <= sig2emu_tp6(0);
test_sig6(9) <= tp_thro_inh(6);
test_sig6(8) <= finor(6);
test_sig6(7) <= ptc2tp6(7);
test_sig6(6) <= ptc2tp6(6);
test_sig6(5) <= ptc2tp6(5);
test_sig6(4) <= ptc2tp6(4);
test_sig6(3) <= ptc2tp6(3);
test_sig6(2) <= ptc2tp6(2);
test_sig6(1) <= ptc2tp6(1);
test_sig6(0) <= ptc2tp6(0);

```

test sig7 : (15:0)

```

eb12 -- PTC 7 testpoints
12 -- DEFINE test_signal(7)
-- DEFINE test_signal(7)
test_signal(7) <= test_sig7;
sig2emu_tp7 <= sig2emu(7);
ptc2tp7 <= ptc2tp(7);
test_sig7(15) <= l1a2front(7);
test_sig7(14) <= en_time_slot(7);
test_sig7(13) <= '0';
test_sig7(12) <= sig2emu_tp7(2); --bcr
test_sig7(11) <= sig2emu_tp7(1); --resync
test_sig7(10) <= sig2emu_tp7(0); --l1a
test_sig7(9) <= tp_thro_inh(7);
test_sig7(8) <= finor(7); -- from FDL
test_sig7(7) <= ptc2tp7(7); -- low_rate
test_sig7(6) <= ptc2tp7(6); -- norm_rate
test_sig7(5) <= ptc2tp7(5); -- random_trig
test_sig7(4) <= ptc2tp7(4); -- test_trig
test_sig7(3) <= ptc2tp7(3); -- cal_trig
test_sig7(2) <= ptc2tp7(2); -- inh_l1a_test
test_sig7(1) <= ptc2tp7(1); -- inh_l1a_cal
test_sig7(0) <= ptc2tp7(0); -- inh_l1a_priv

```