

VME-CHIP-TCS

ADDR_DEC_TCS

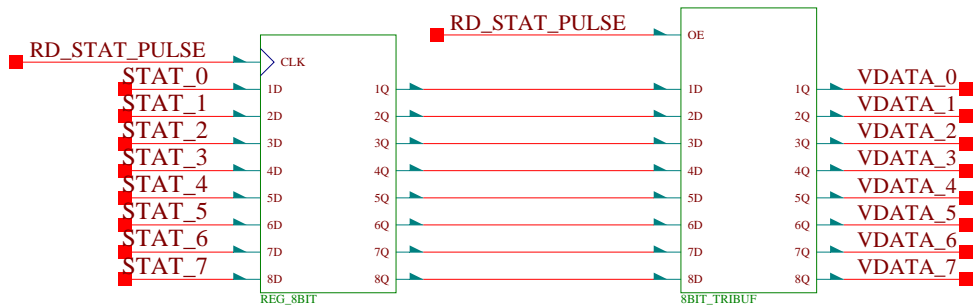
Version: **V1.1**

HEPHY VIENNA
ELEKTRONIK 1

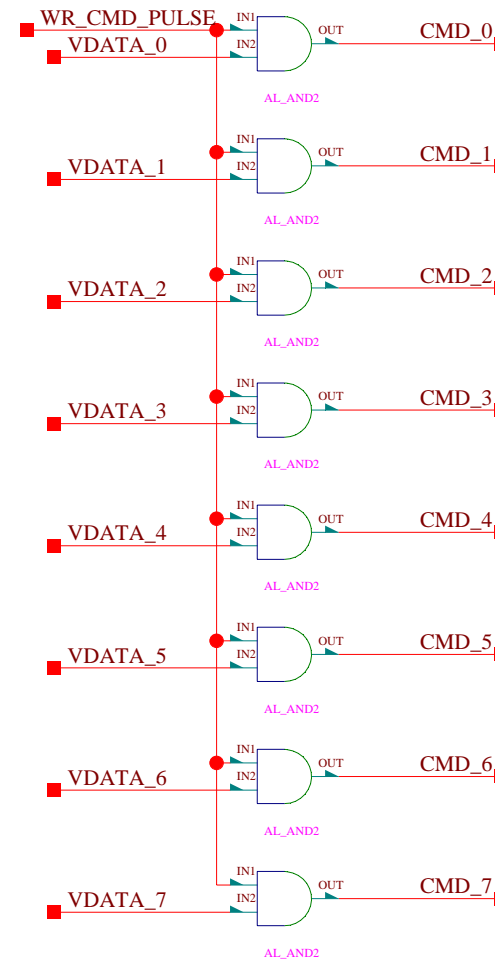
sheet **1** of **1**

modified by: HB 2-27-2007_13:40

checked by: CHECKER 0-00-0000_00:00



VDATA_[7:0]



VME-CHIP

GEN_PULSE_REG

Version: **V2.0**

HEPHY VIENNA
ELEKTRONIK 1

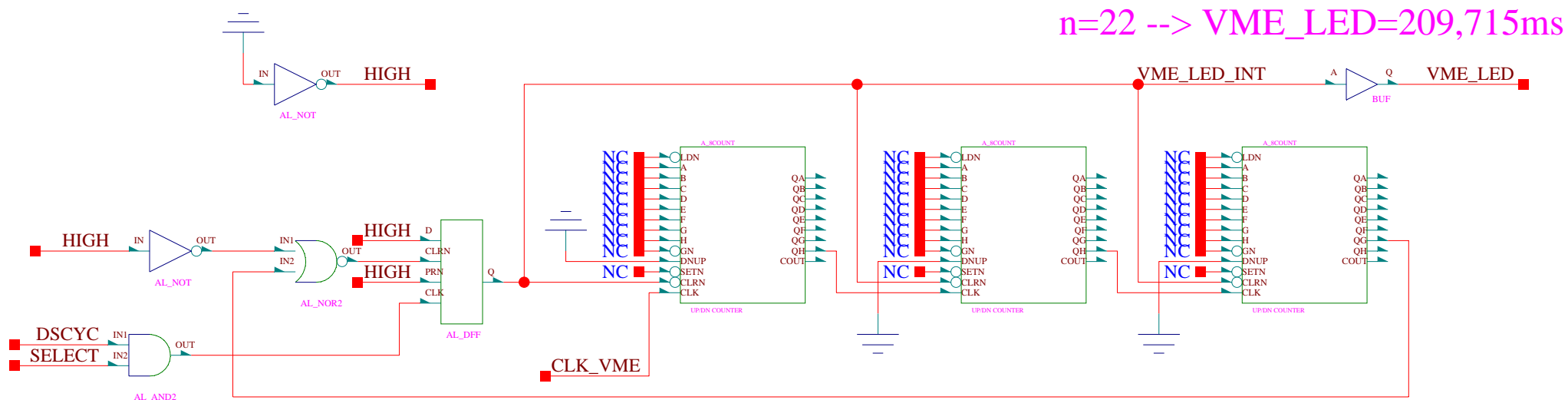
sheet **1** of **1**

modified by: HB

9-1-2005_10:29

checked by: CHECKER

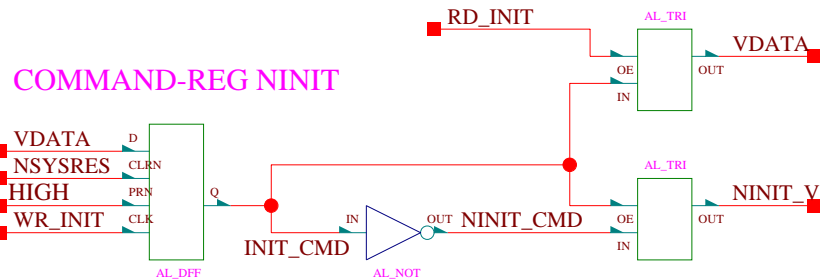
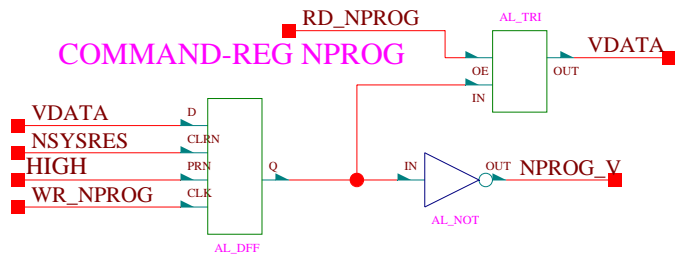
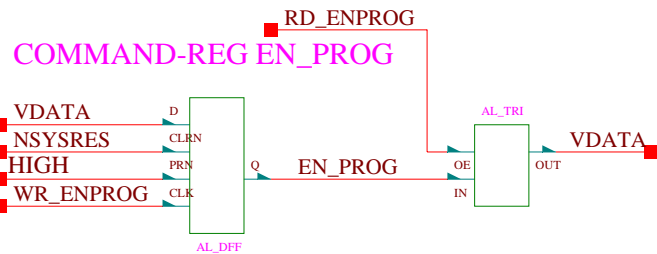
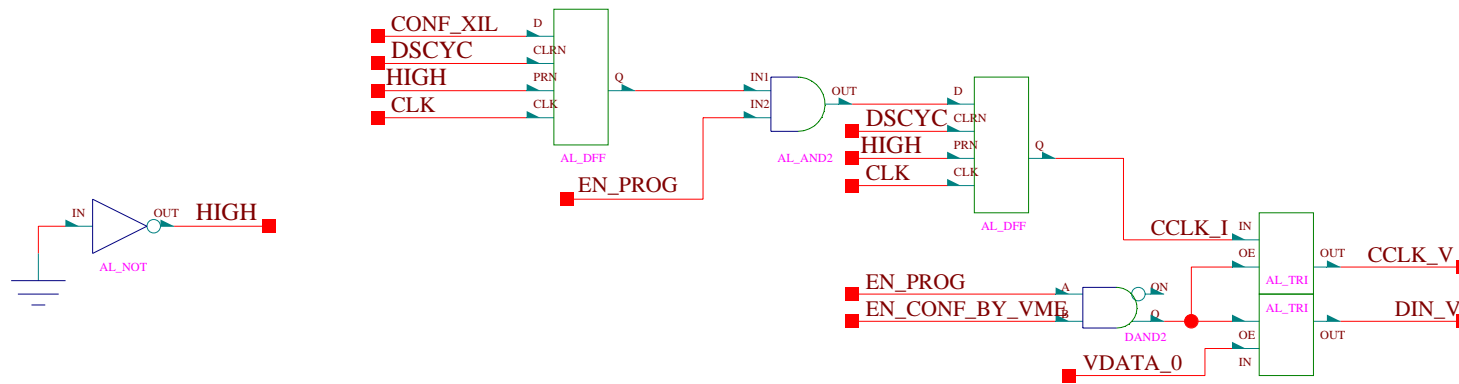
0-00-0000_00:00



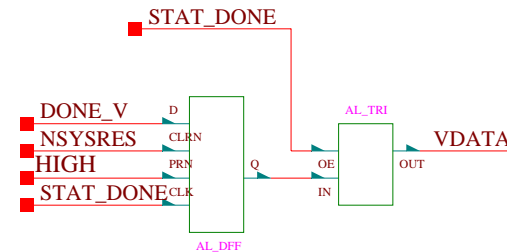
Formel: $(2^{n+1}-1) \cdot 25\text{ns}$ ($25\text{ns}=\text{CLK_VME}$)

<h1 style="margin: 0;">VME-CHIP</h1>	
<h2 style="margin: 0;">LED_DELAY</h2>	
Version:	V2.0
HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 1
modified by: HB	9-1-2005_10:32
checked by: CHECKER	0-00-0000_00:00

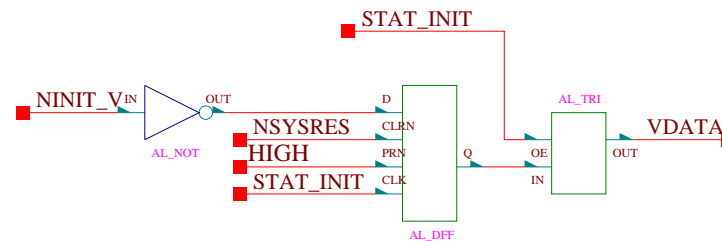
CONFIGURATION OF XILINX CHIP (CCLK, DIN)



STATUS-REG DONE



STATUS-REG NINIT



VME-CHIP XILINX_CONF

Version: **V2.0** Configuration

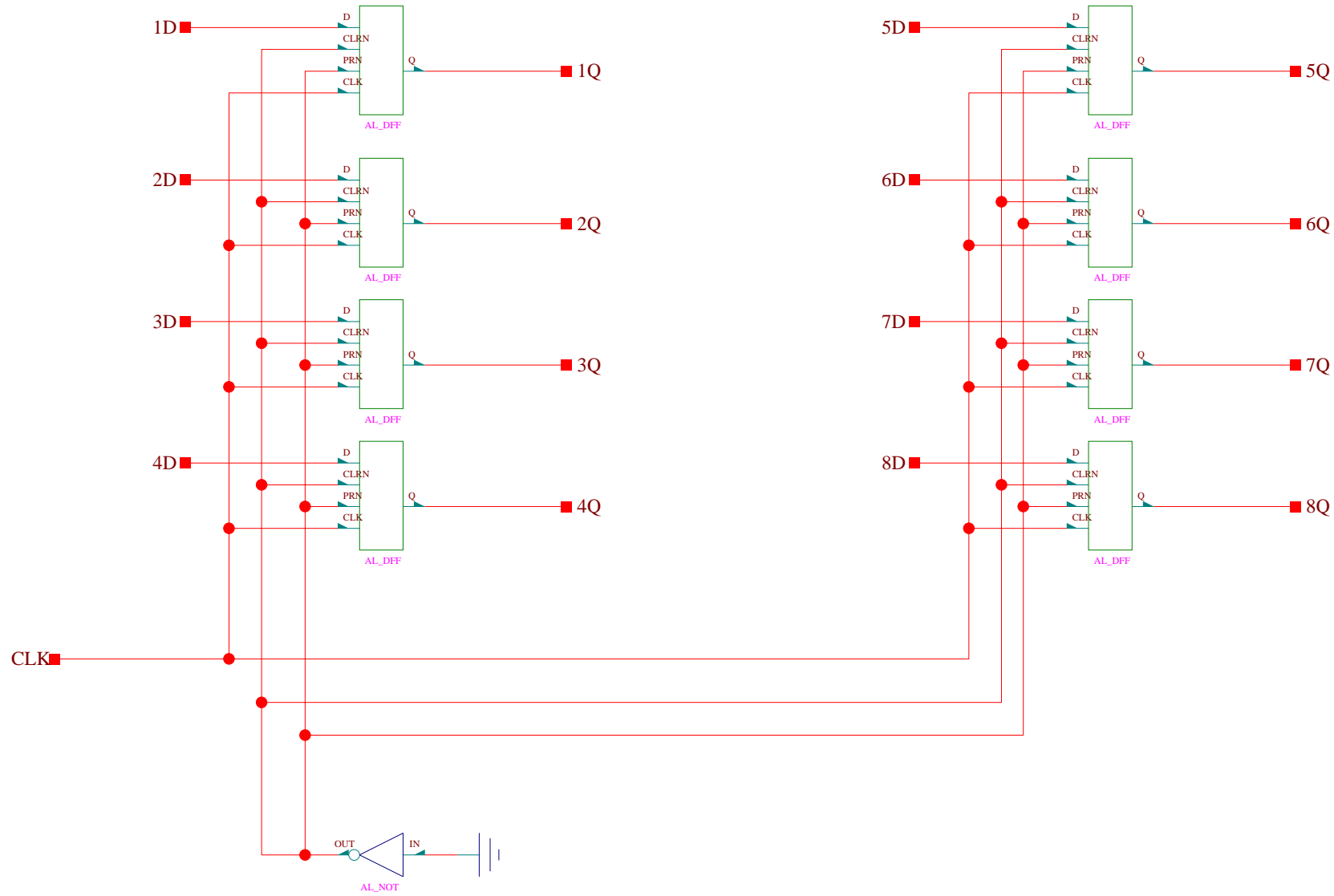
HEPHY VIENNA
ELEKTRONIK 1 sheet **1** of **1**

modified by HB 8-26-2005_14:23

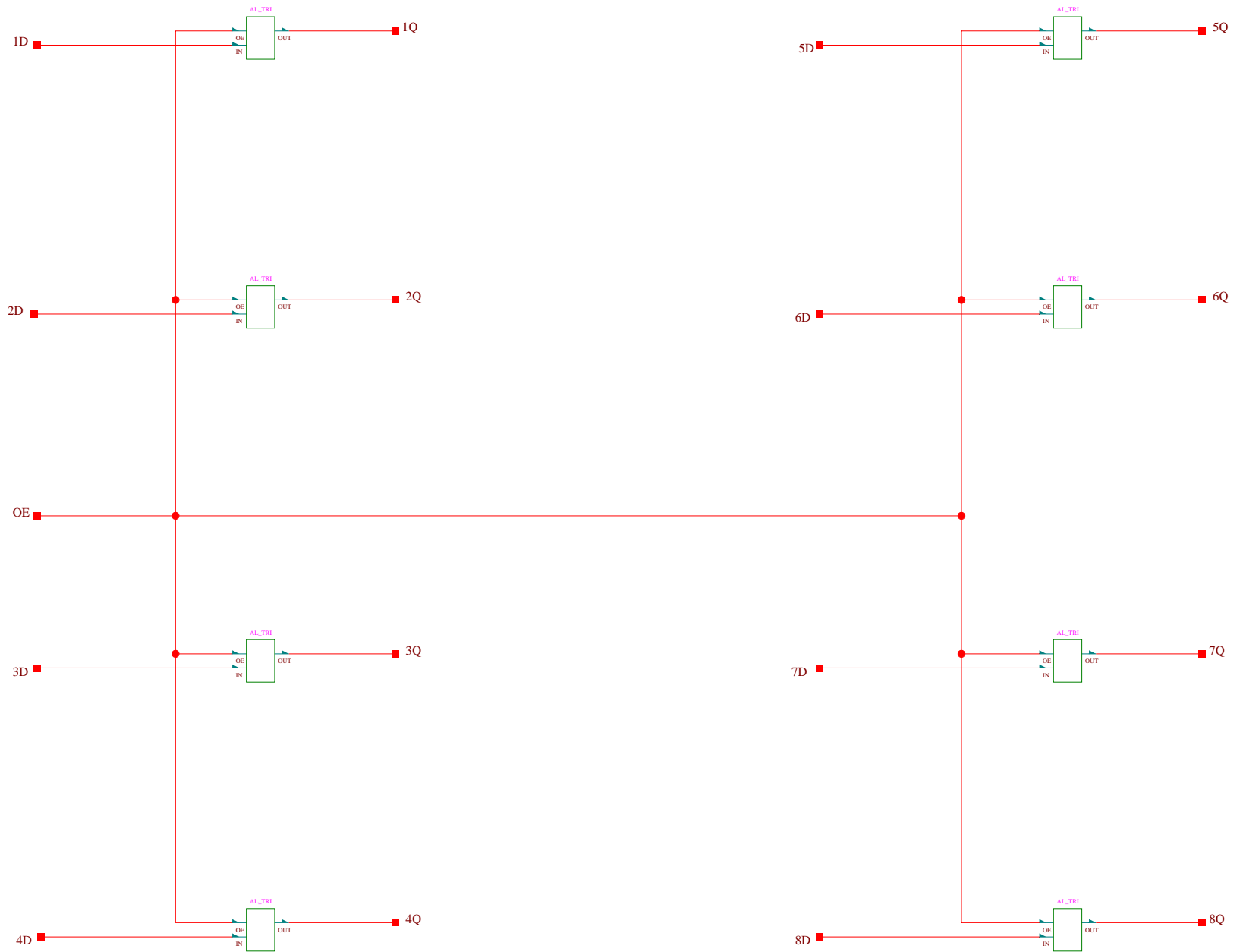
checked by: CHECKER 0-00-0000_00:00

reg_8bit

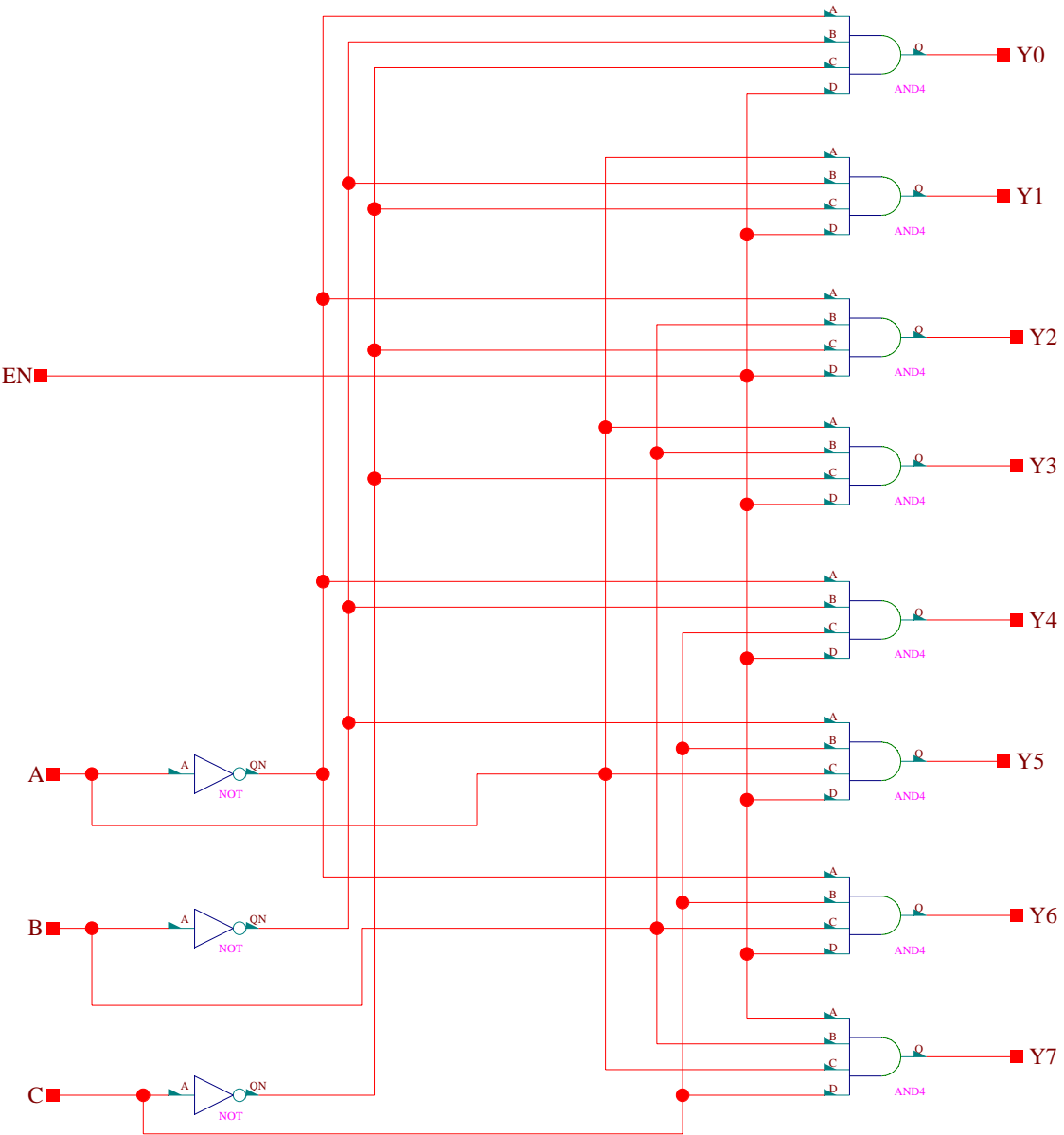
8-bit register generated by LAB3



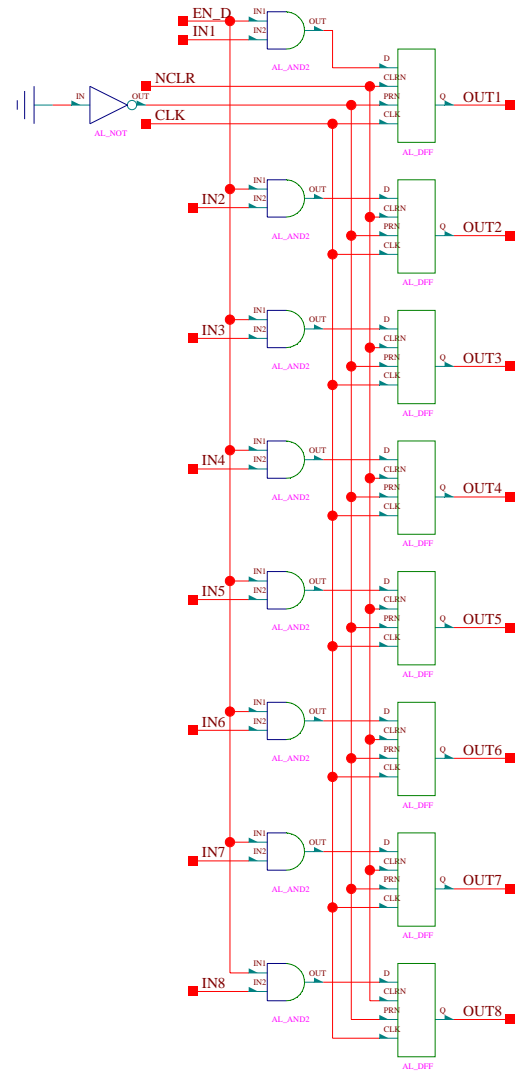
8bit_tribuf



decoder_3to8



reg_8bit_en_d



```
-----
--
-- LOGIC CORE: vme-chip logic
-- MODULE NAME: chip_id_version
-- INSTITUTION: Hephy Vienna
-- DESIGNER: H. Bergauer
--
-- VERSION: V2.0
-- DATE: 08 2005
--
-- FUNCTIONAL DESCRIPTION:
-- chip_id and version register (read only)
--
-----
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
LIBRARY altera;
USE altera.maxplus2.ALL;

USE work.constant_pkg.ALL;

ENTITY chip_id_version IS
    PORT(
        VDATA      : INOUT STD_LOGIC_VECTOR(7 DOWNTO 0);
        CARD_NR     : IN     STD_LOGIC_VECTOR(3 DOWNTO 0);
        CHIP_ID     : IN     STD_LOGIC_VECTOR(3 DOWNTO 0);
        VERSION     : IN     STD_LOGIC_VECTOR(3 DOWNTO 0));
END chip_id_version;

ARCHITECTURE rtl OF chip_id_version IS

    -- CONSTANT for card_name and version defined in working-dir\vhdl !!!

    SIGNAL chip_id_value : std_logic_vector(31 downto 0);
    CONSTANT cms_gt: STD_LOGIC_VECTOR(15 DOWNTO 0) := X"0001"; -- fixed code for GT-system
    -- card_nr will be delivered from VME64x-chip, HB250805
    CONSTANT chip_name: STD_LOGIC_VECTOR(3 DOWNTO 0) := X"2"; -- fixed code for chip_name
    CONSTANT chip_nr: STD_LOGIC_VECTOR(3 DOWNTO 0) := X"1"; -- fixed code for chip_nr = 0x

BEGIN
    chip_id_value <= cms_gt & card_name & card_nr & chip_name & chip_nr;

    -- chip_id and version register (read only)
    tri_chip_id_3:
    FOR i IN 0 TO 7 GENERATE
        call_chip_id_3: tri
            PORT MAP(chip_id_value(i+24),
                chip_id(3),
                vdata(i));
    END GENERATE tri_chip_id_3;

    tri_chip_id_2:
    FOR i IN 0 TO 7 GENERATE
        call_chip_id_2: tri
            PORT MAP(chip_id_value(i+16),
                chip_id(2),
                vdata(i));
    END GENERATE tri_chip_id_2;

    tri_chip_id_1:
    FOR i IN 0 TO 7 GENERATE
        call_chip_id_1: tri
            PORT MAP(chip_id_value(i+8),
                chip_id(1),
                vdata(i));
    END GENERATE tri_chip_id_1;

    tri_chip_id_0:
```

```
FOR i IN 0 TO 7 GENERATE
  call_chip_id_0: tri
  PORT MAP(chip_id_value(i),
    chip_id(0),
    vdata(i));
END GENERATE tri_chip_id_0;

tri_version_3:
FOR i IN 0 TO 7 GENERATE
  call_version_3: tri
  PORT MAP(version_value(i+24),
    version(3),
    vdata(i));
END GENERATE tri_version_3;

tri_version_2:
FOR i IN 0 TO 7 GENERATE
  call_version_2: tri
  PORT MAP(version_value(i+16),
    version(2),
    vdata(i));
END GENERATE tri_version_2;

tri_version_1:
FOR i IN 0 TO 7 GENERATE
  call_version_1: tri
  PORT MAP(version_value(i+8),
    version(1),
    vdata(i));
END GENERATE tri_version_1;

tri_version_0:
FOR i IN 0 TO 7 GENERATE
  call_version_0: tri
  PORT MAP(version_value(i),
    version(0),
    vdata(i));
END GENERATE tri_version_0;

END ARCHITECTURE rtl;
```

constant_pkg.vhd

27.02.2007

```
--  
-- This is the definition of card_name (of chip_id) and version  
-- for TCS-9U - VME chip - V1009  
--  
LIBRARY ieee;  
USE ieee.std_logic_1164.ALL;  
PACKAGE constant_pkg IS  
  
--      chip_id_value is made in CHIP_ID_VERSION.vhd !!!  
      CONSTANT card_name: STD_LOGIC_VECTOR(3 DOWNTO 0) := X"5"; -- TCS-9U-card => 0x5  
      CONSTANT version_value: STD_LOGIC_VECTOR(31 DOWNTO 0) := X"00001009";  
  
END constant_pkg;
```

```
-----  
--  
-- LOGIC CORE: TIM-module vme-chip logic  
-- MODULE NAME: opdr_vhdl  
-- INSTITUTION: Hephy Vienna  
-- DESIGNER: H. Bergauer  
--  
-- VERSION: V1.0  
-- DATE: 08 2005  
--  
-- FUNCTIONAL DESCRIPTION:  
-- open-drain buffer  
--  
-----  
LIBRARY ieee;  
USE ieee.std_logic_1164.ALL;  
LIBRARY altera;  
USE altera.maxplus2.ALL;  
  
ENTITY opdr_vhdl IS  
    PORT(  
        IP : IN    STD_LOGIC;  
        OP : INOUT STD_LOGIC);  
END opdr_vhdl;  
  
ARCHITECTURE rtl OF opdr_vhdl IS  
BEGIN  
  
    inst_opndrn: OPNDRN  
    PORT MAP(ip, op);  
  
END ARCHITECTURE rtl;
```